Status of Data Acquisition at Belle

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for Belle DAQ subgroup
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Outline

1. Introduction
2. Data flow
   - Detector readout
   - Event building farm
   - Data recording system
3. DAQ inefficiency
4. Run control and Data monitoring
5. Upgrade plan
6. Summary

1. Introduction

Design Performance:

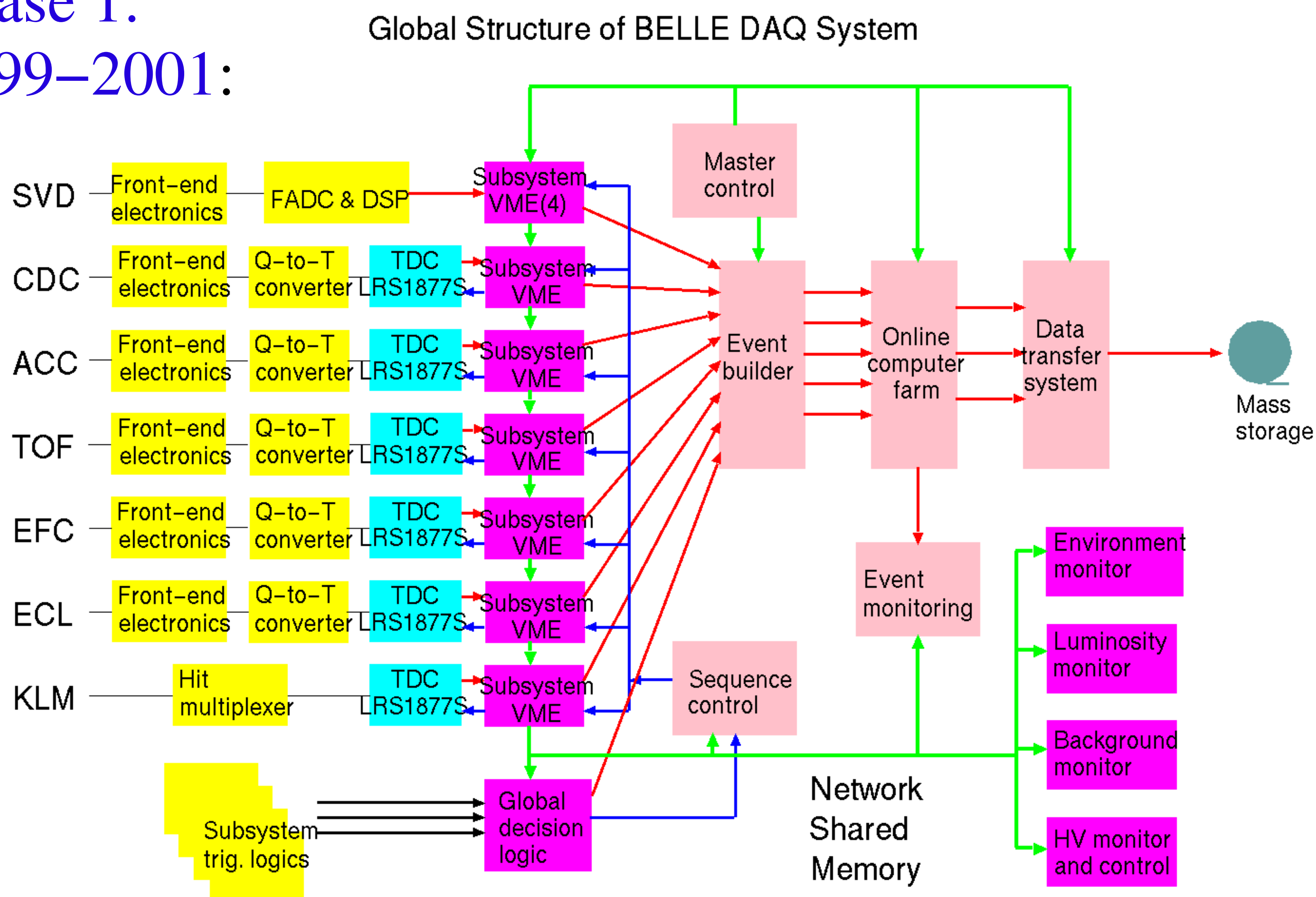
- Trigger rate : 200Hz (typical), 500Hz(max)
- Deadtime < 10% at 500Hz
- Data size : ~30KB/event
- Recording speed : 5MB/sec (typical) 15MB/sec(max)

Design Policy:

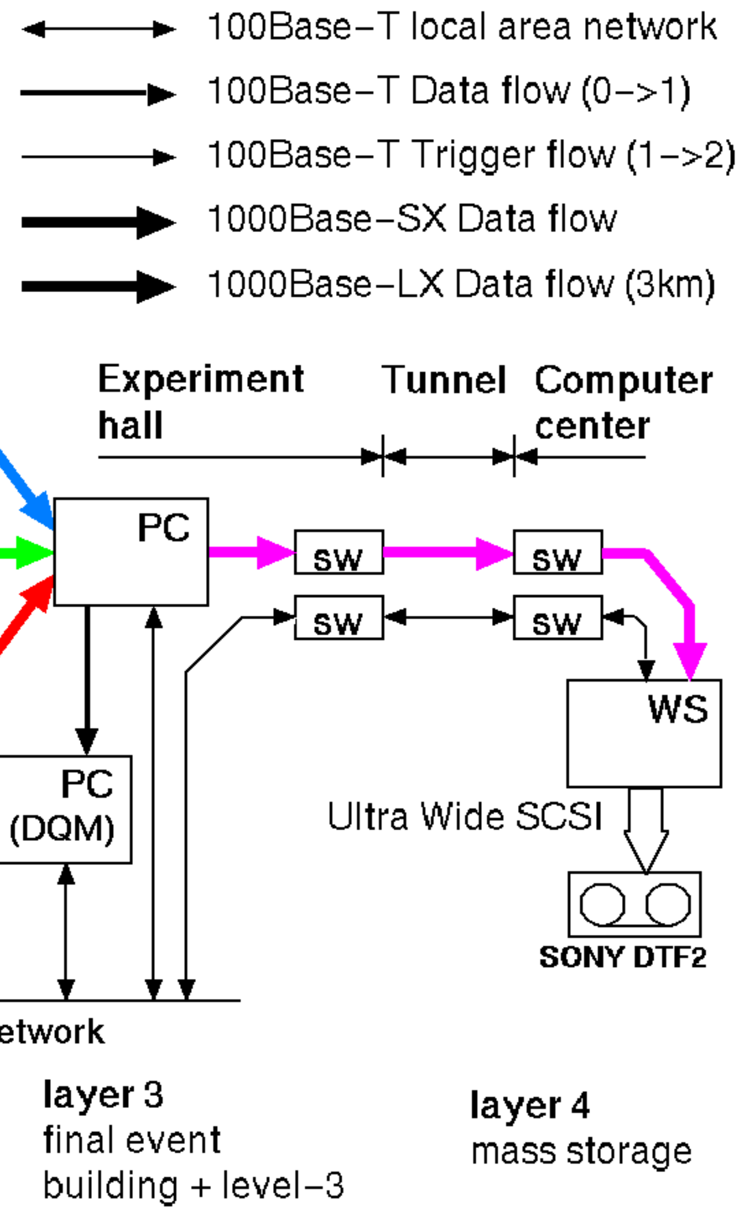
* We do not use pipelined readout system
  –> it was difficult to build due to rack of man–power/money
* "Delay and Gate" readout scheme is used
  <– very common in fixed target experiments
* Use "commodities" as much as possible
  (especially in down stream of data flow)
* Single stream output (no parallel I/O, no OODB)

2. Data flow

Phase 1:
1999–2001:



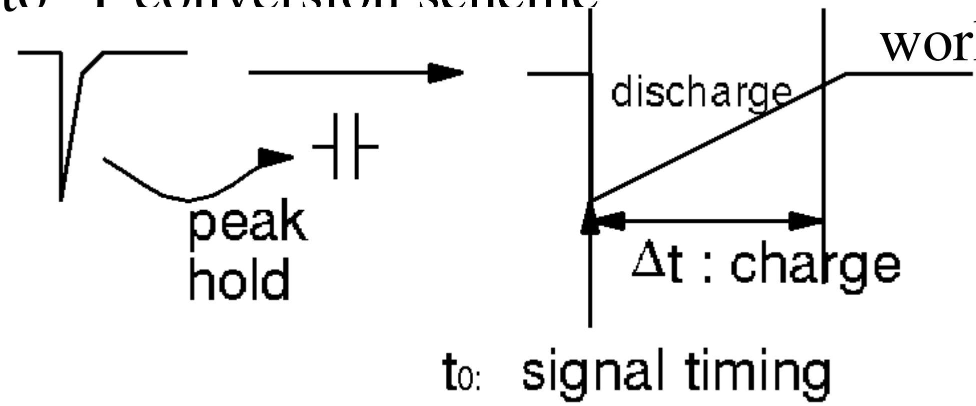
Phase 2: 2001–



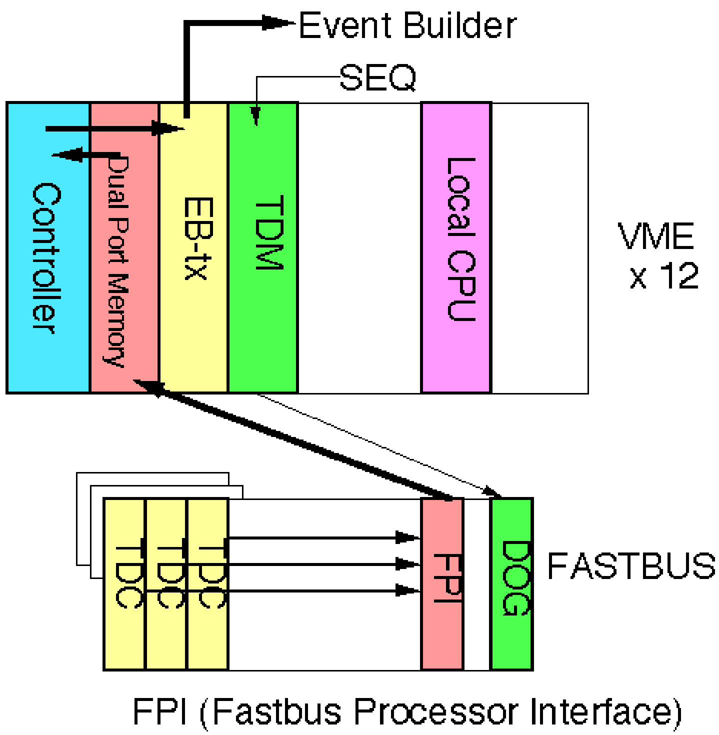
PC: SMP server with 4 CPUs

Frontend Readout (except SVD)

– Q–to–T conversion scheme



Q–to–T : LeCroy MQT300
multi–hit TDC : LRS1877S

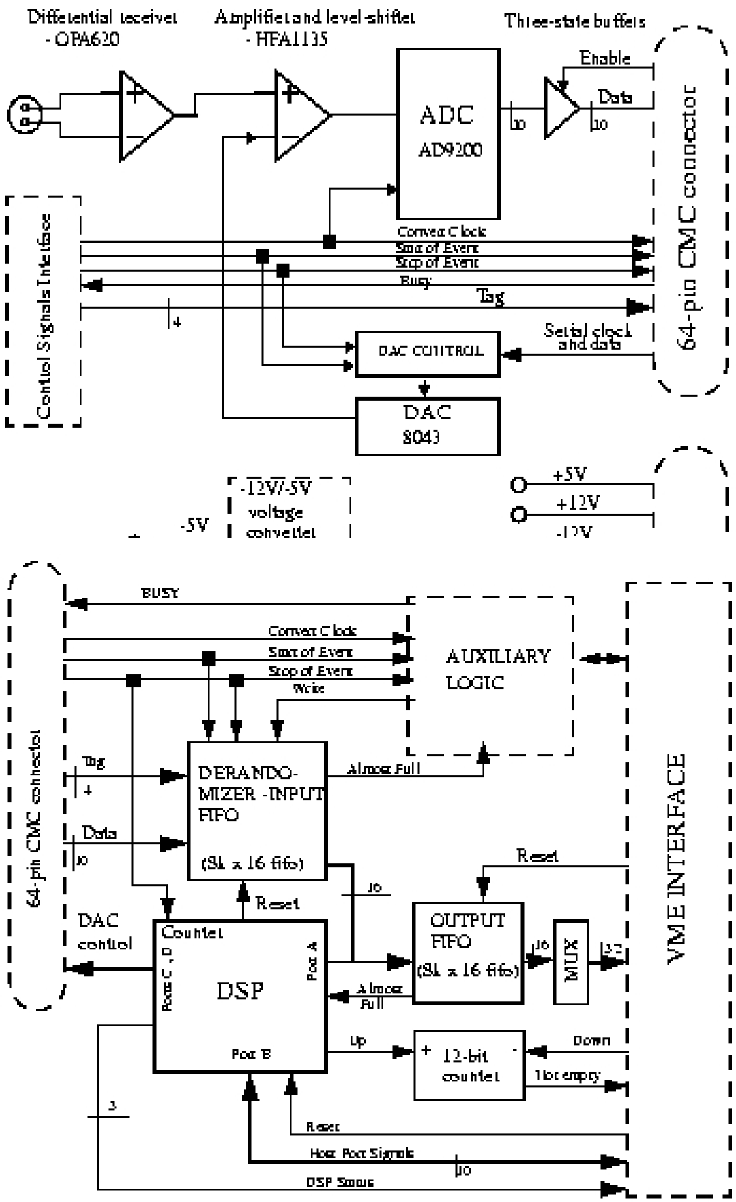


* TDC: FASTBUS based
– operated in common stop
(except ECL)

* Data transfer to VME
– Home grown product
(a kind of reflective memory)

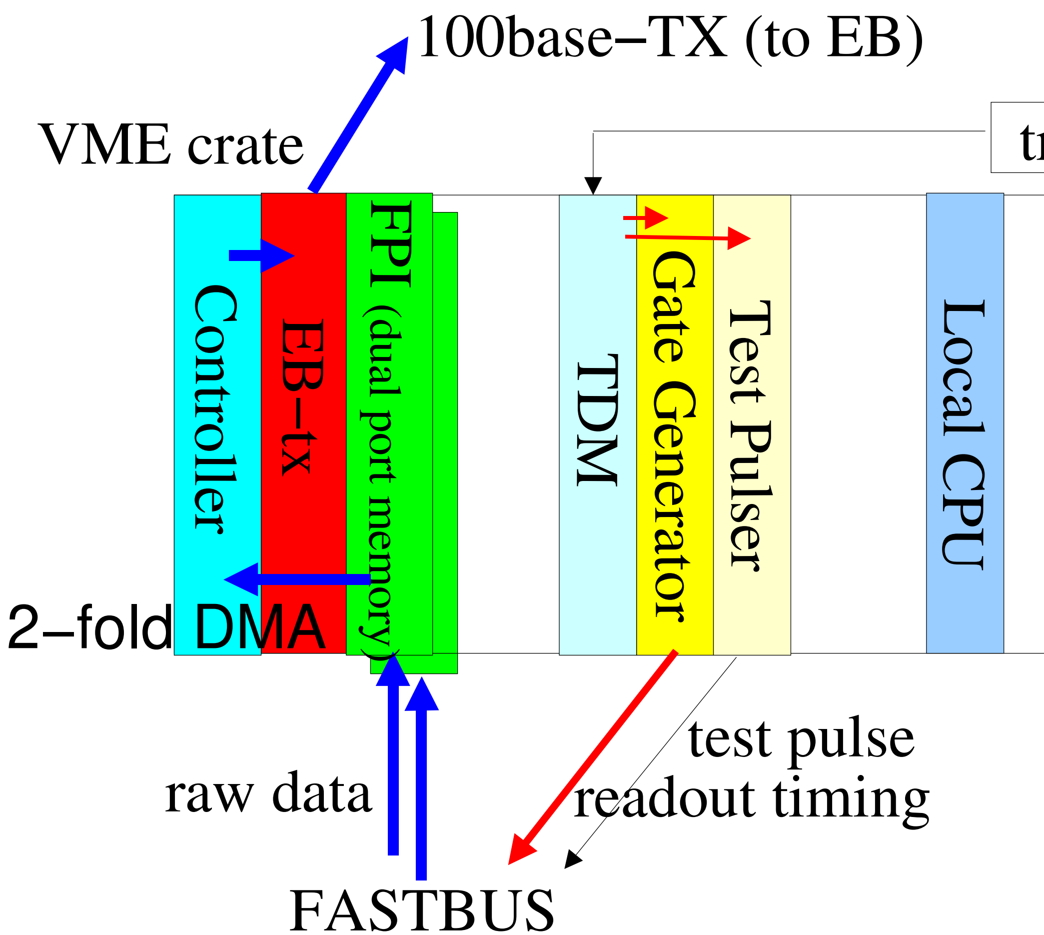
Frontend Readout for SVD

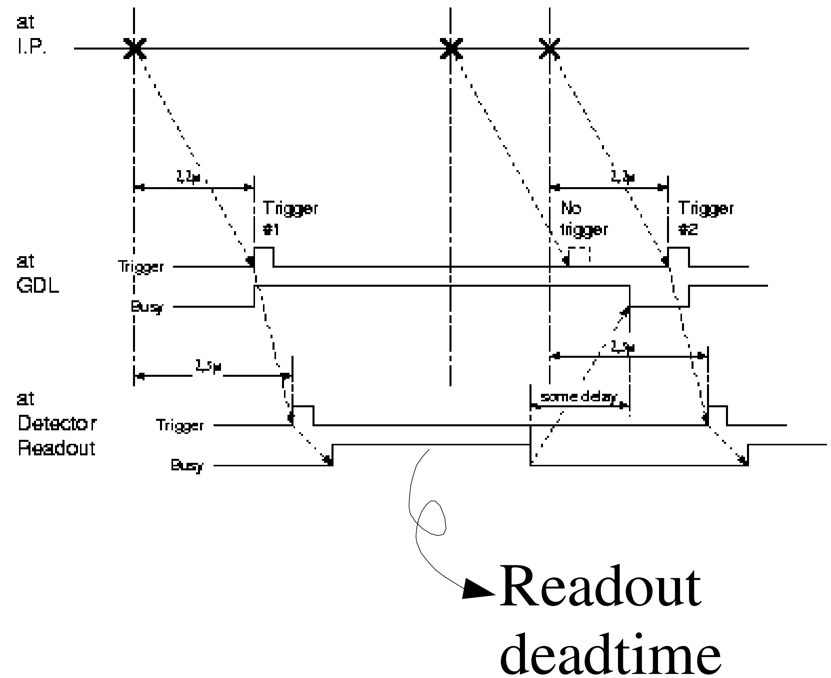
"HALNY" module : FADC + DSP



* Designed to read out VA chip
* No data sparcification in VA chip
* Zero suppression by DSP

Readout Subsystem





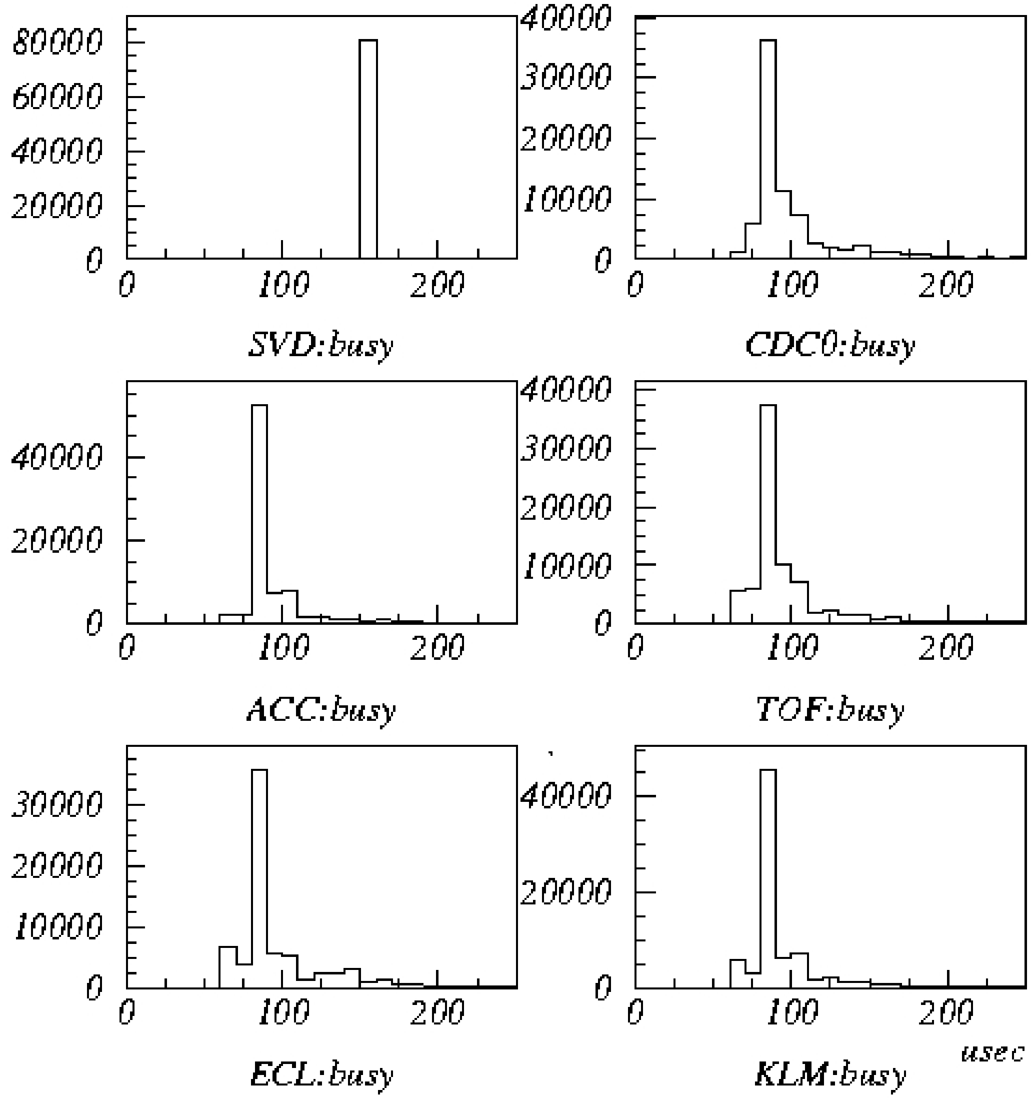
* Readout timing : TDM (Timing Distributor Module)

– receive trigger signal and generate readout timing

* Data transfer: Controller module (MVME162 controlled by VxWorks)

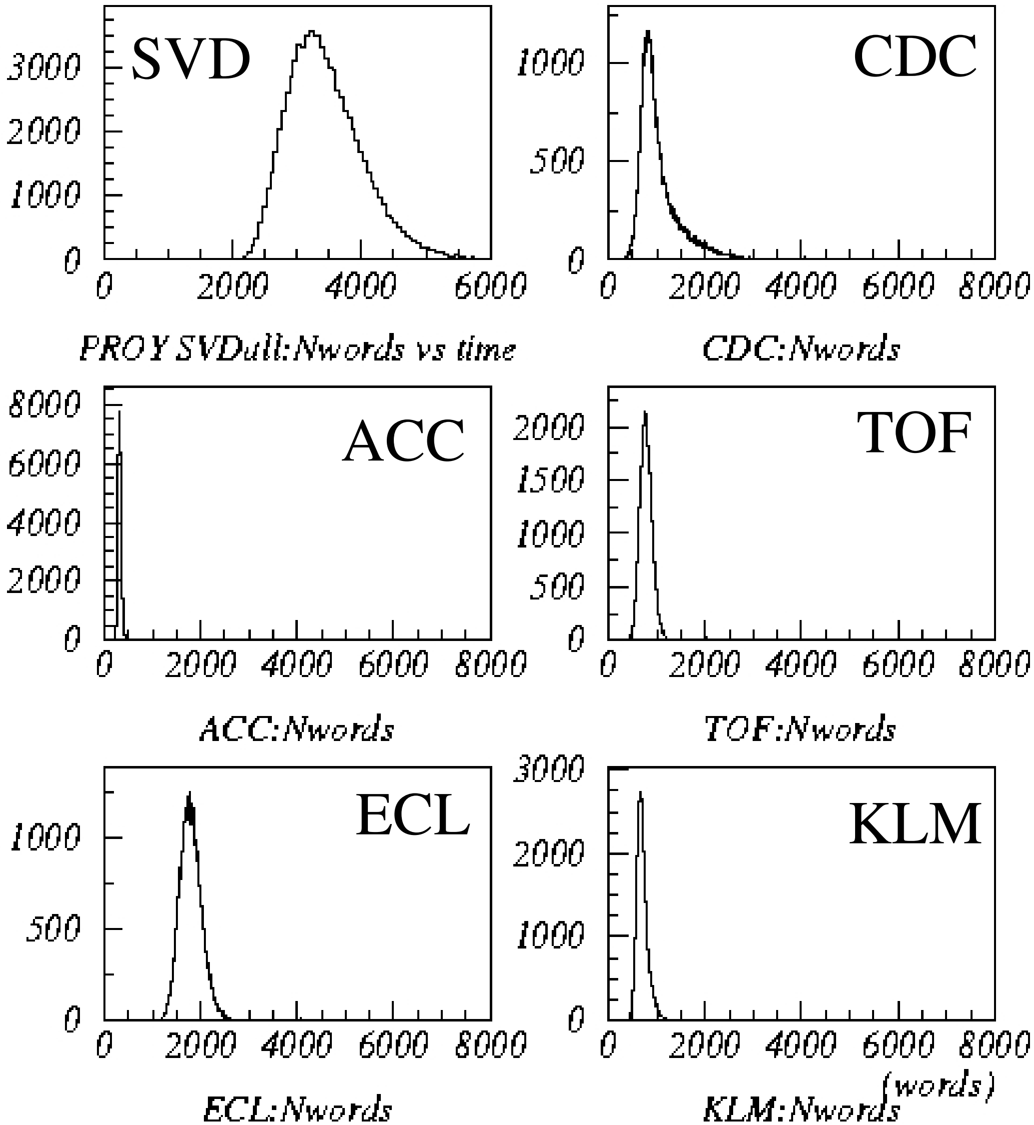
– sub–event bulding for the detector

Distribution of "busy" time



Typical deadtime:
FASTBUS : ~ 80μsec
SVD: ~ 160μsec

Distribution of No. of words for each detector



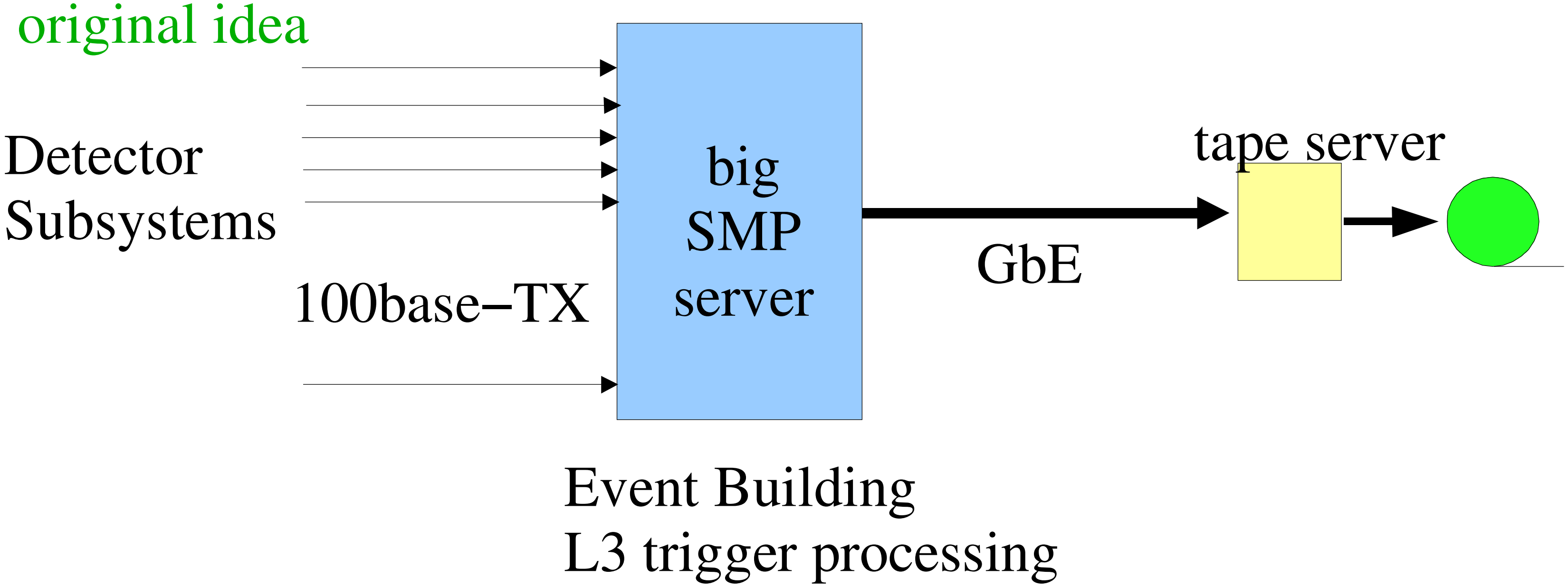
* SVD
  - 4 VME subsystems are used for readout.

Average event size:

SVD: ~ 15KB
CDC: ~ 4KB
ACC: ~ 1KB
TOF: ~ 2KB
ECL: ~ 8KB
KLM: ~ 3KB
TRG: ~ 3KB
(ZCDC: ~ 2KB)

Switchless Event Building

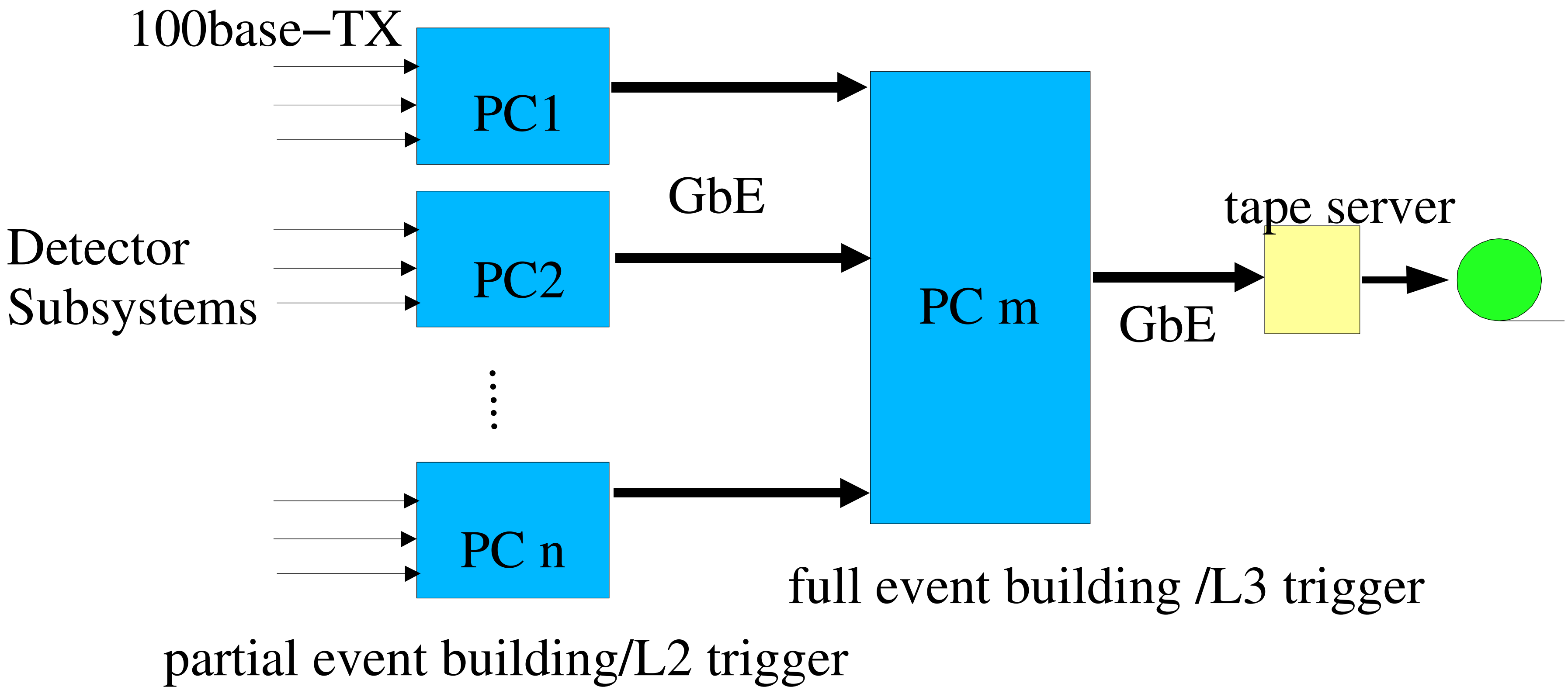
* original idea



– Exactly the same offline environment –> easy to write L3 code
 <– BASF supports parallel processing on SMP
– Event building –> trivial using "Panther" on shared memory
 (just a matter of handling pointers on shared mem.)

* a large scale SMP server –> expensive
* bandwidth of CPU bus for SMP can be bottleneck
* need to drive too many network cards by single OS –> reliable?

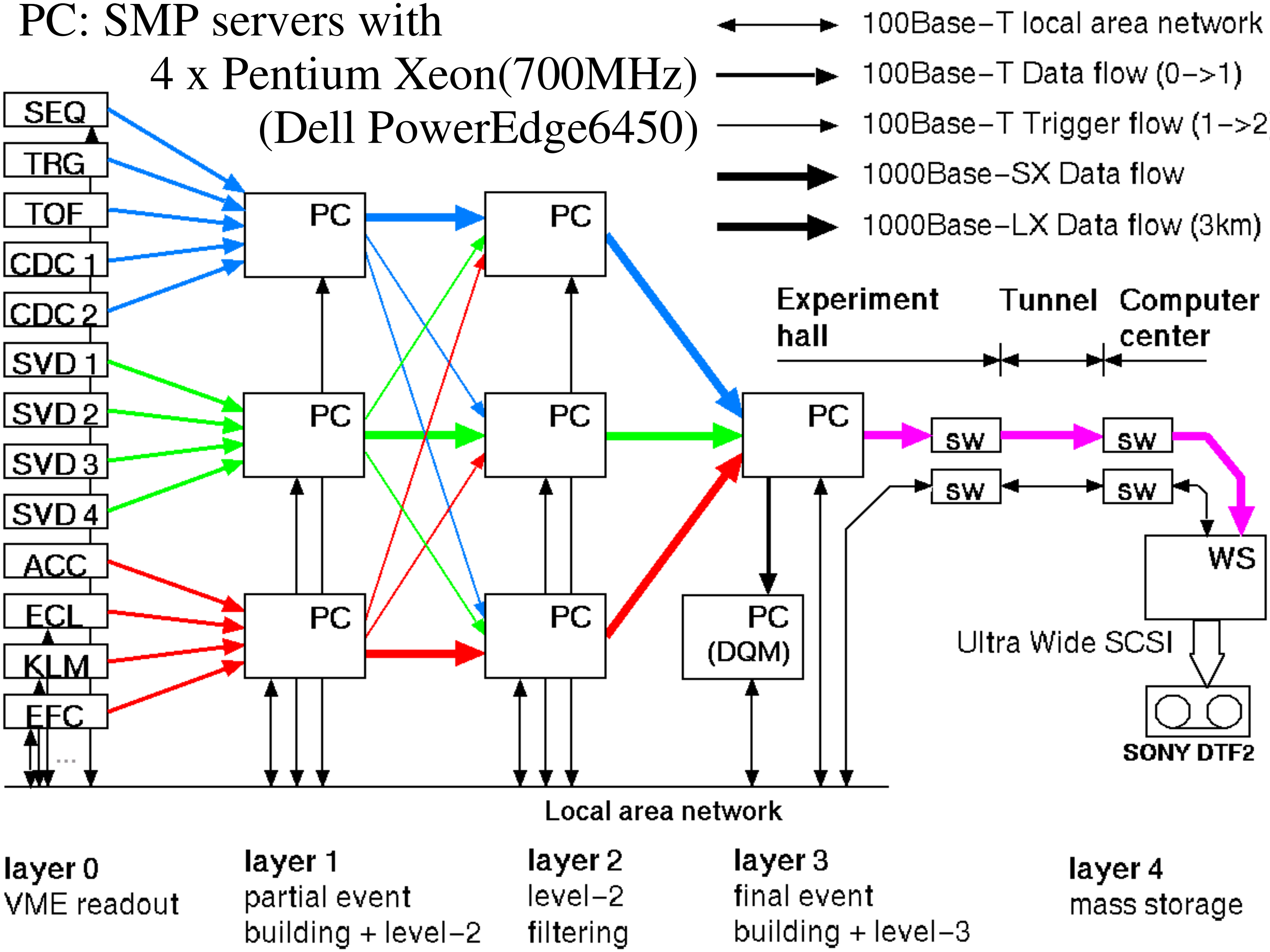
Multi–step event building



* Step–by–step event building
* Enable to use small scale PCs –> low cost
* Level 2 trigger: efficient data reduction in upper stream
* distribution of processing power to multiple PCs –> scalability

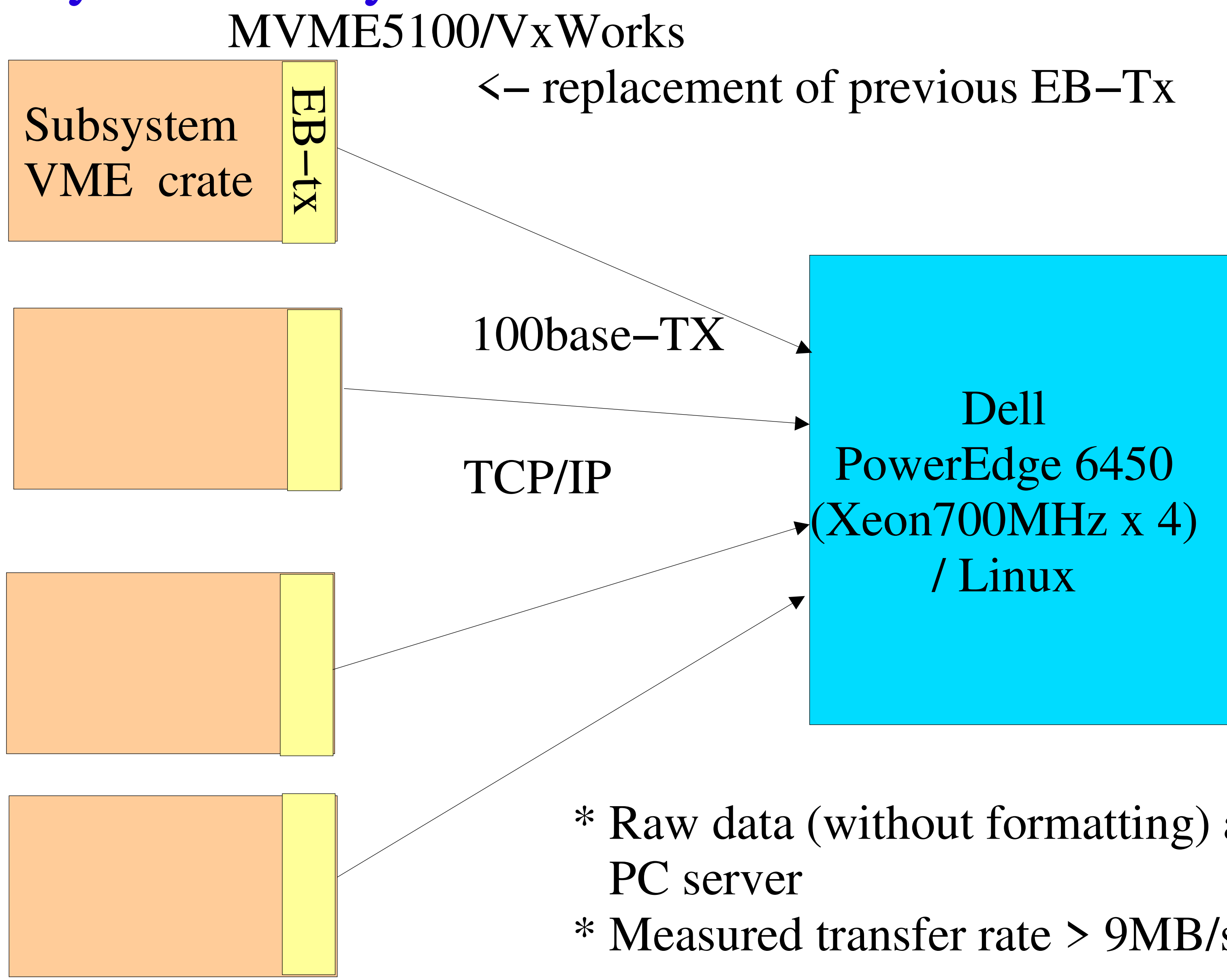
* point–to–point network connection
  –> can avoid traffic control problem

PC: SMP servers with
4 x Pentium Xeon(700MHz)
(Dell PowerEdge6450)



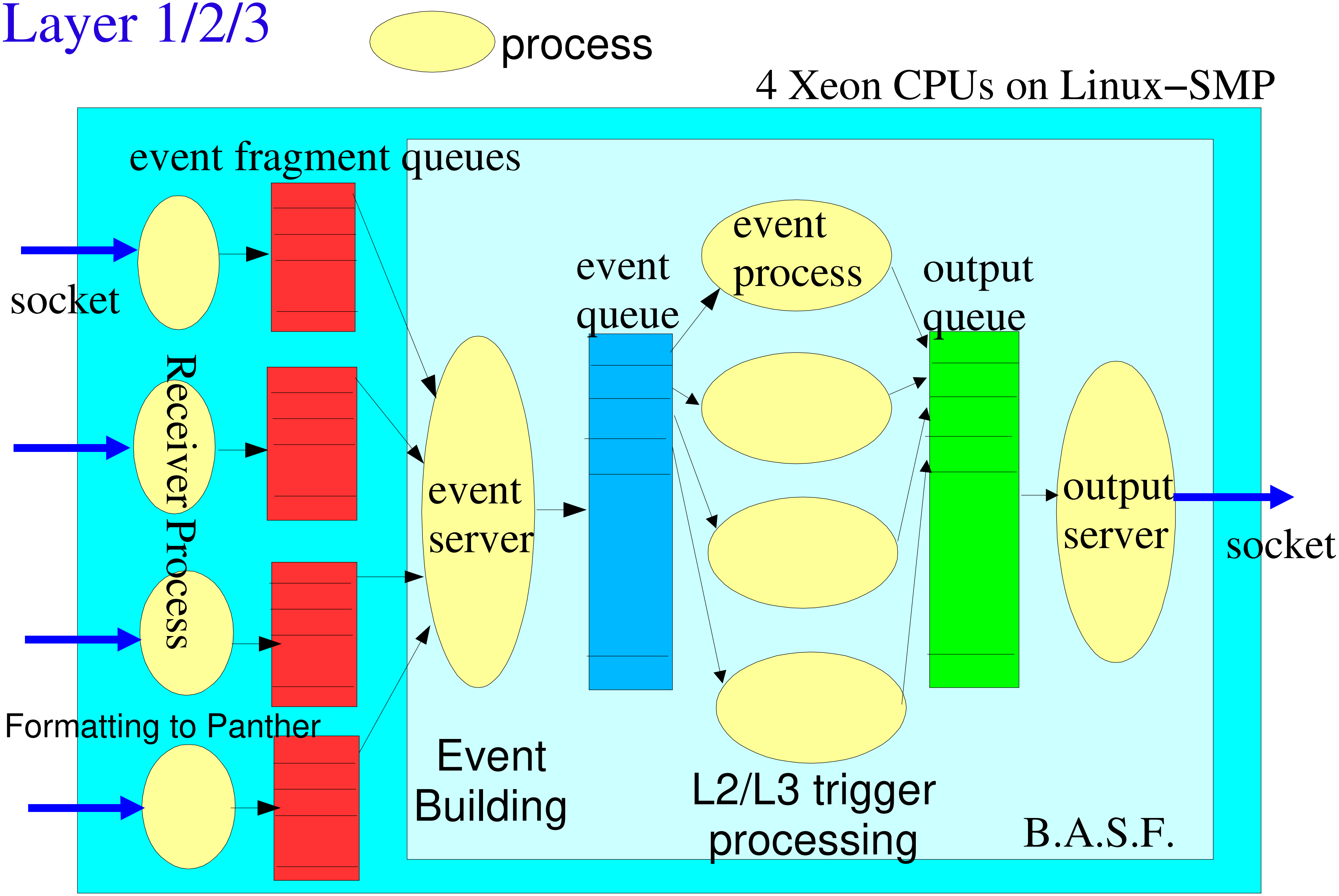
OS: Linux Data transfer : TCP/IP socket connection

Layer0 –> Layer1



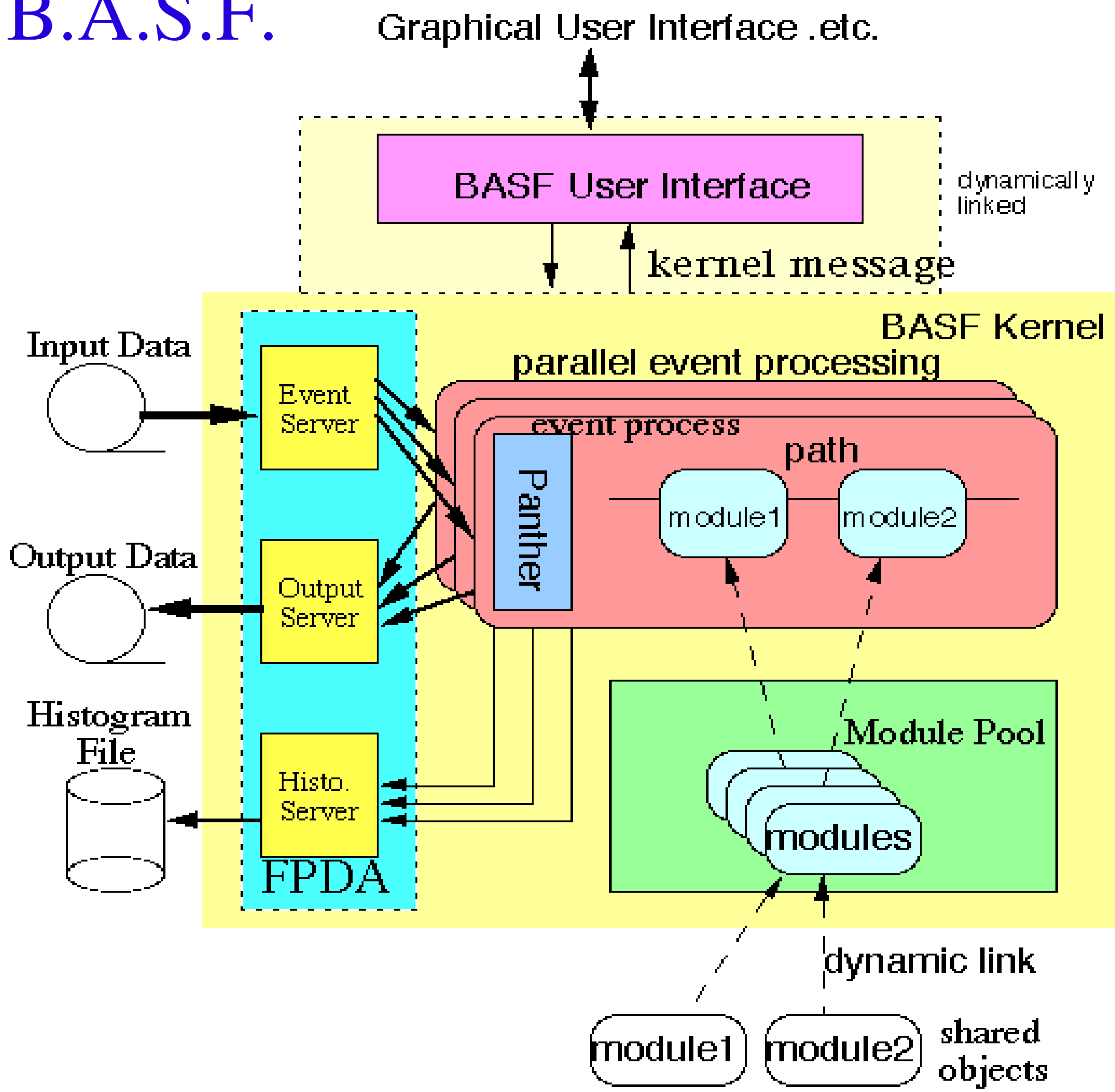
* Raw data (without formatting) are sent to PC server
* Measured transfer rate > 9MB/sec

Layout 1/2/3



L3 reduction rate : ~ 0.5

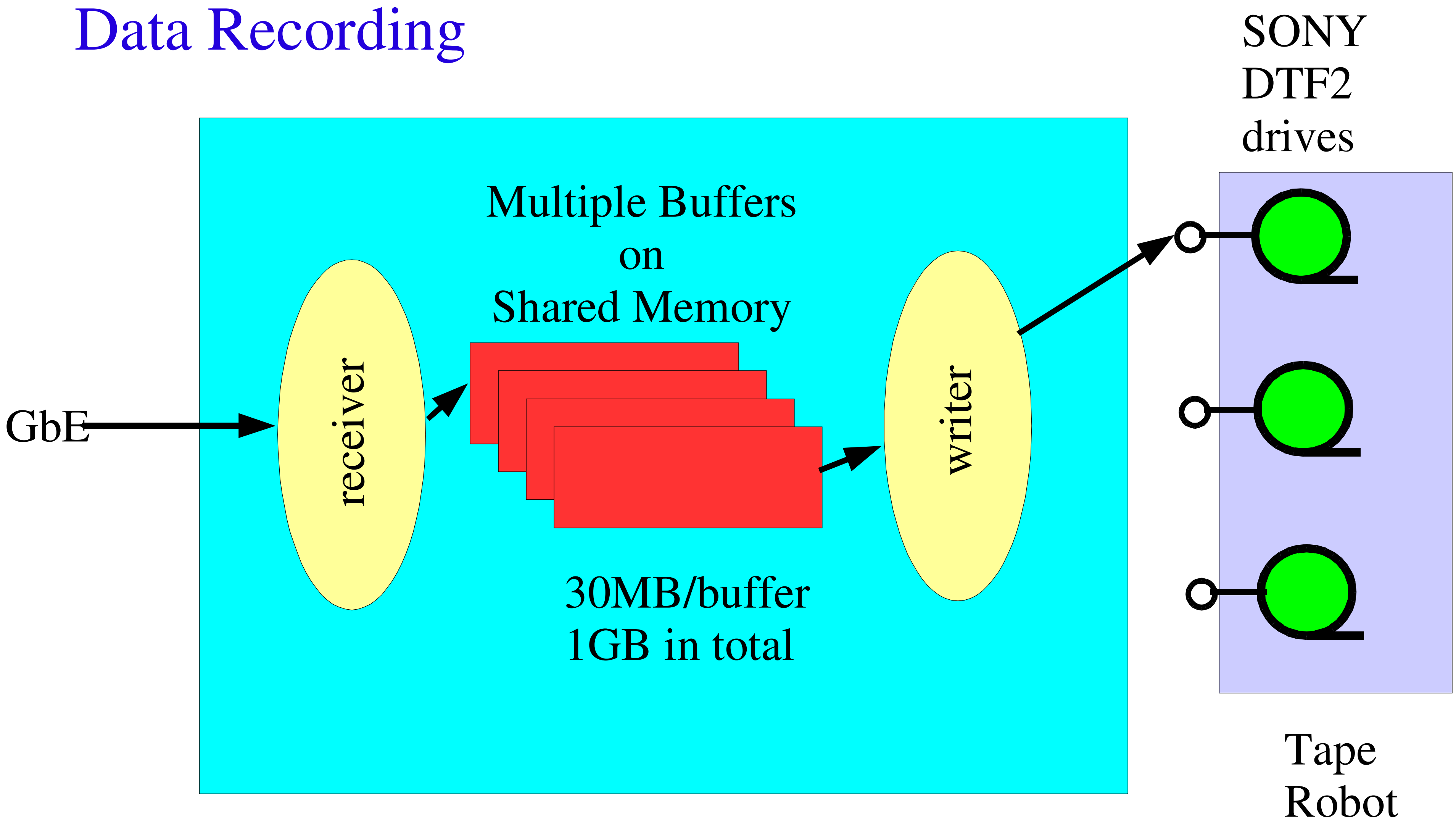
B.A.S.F.



* event process:
 separate UNIX process
–> parallel event–by–event
 processing on SMP

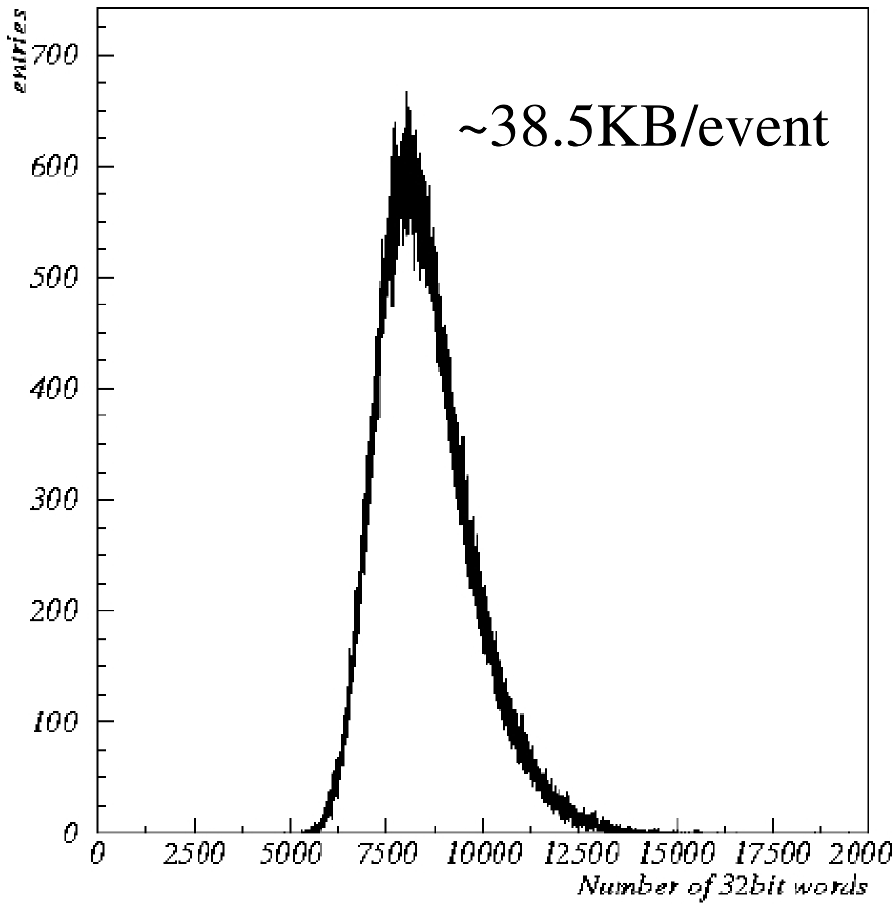
* analysis modules and
 I/O packages are
 dynamically linked

Data Recording

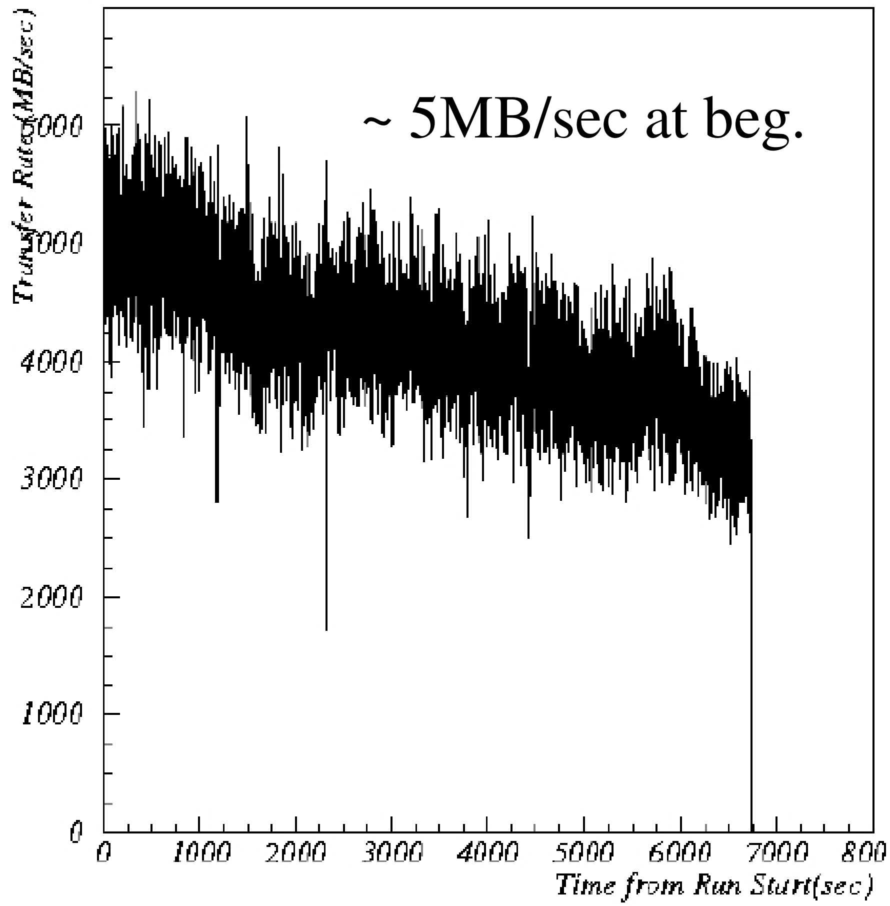


DTF2: Digital vide tape drive
writing speed : 24MB/sec

No. of words at recorder



Transfer rate vs time



– After L3 trigger reduction(~120Hz at recorder)

Measured performance

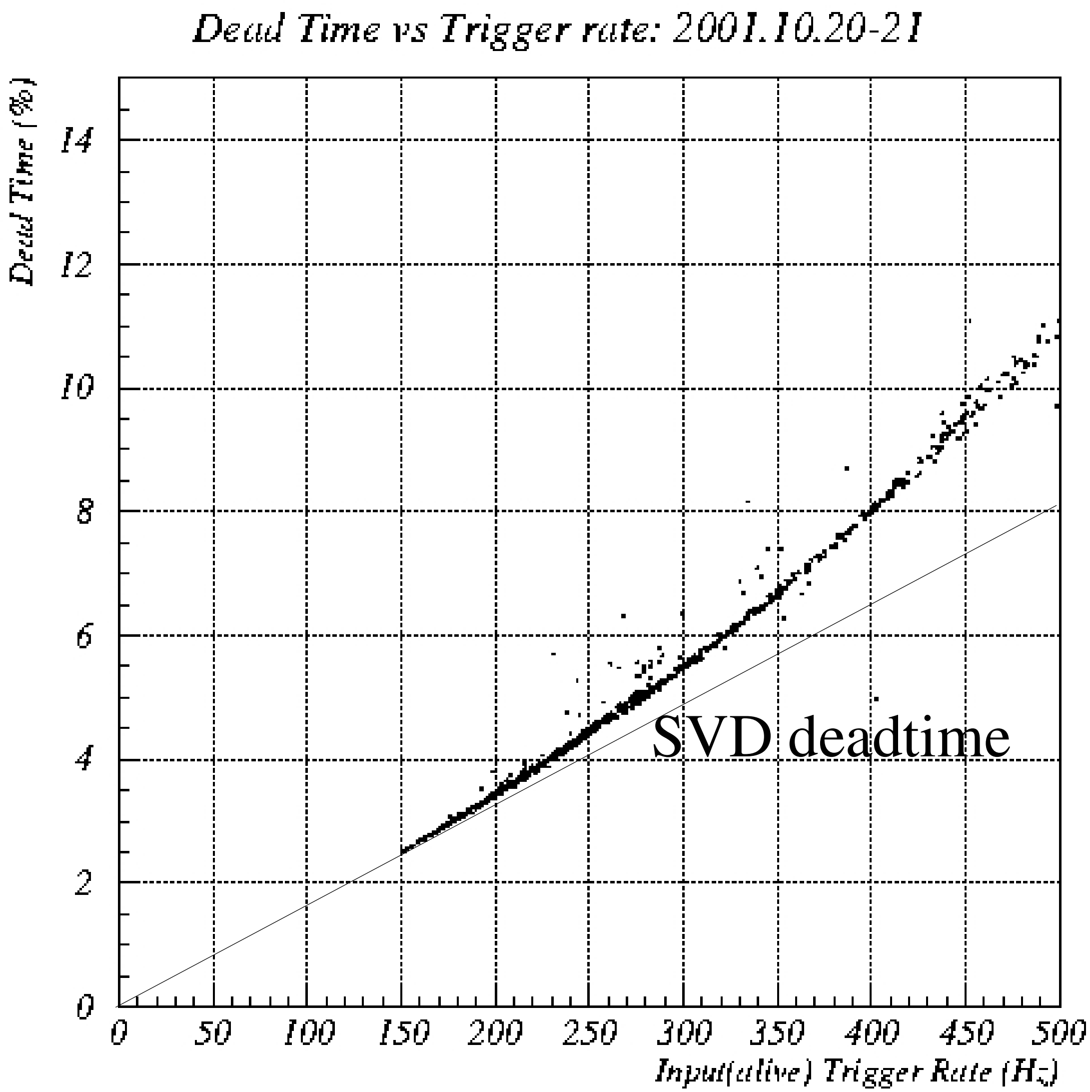
- point–to–point transfer speed on GbE : > 70MB/sec

- Overall speed:
  - – dummy events on layer 1 node –> tape
  - – event building on layer 1 and layer 3
  - – no event filtering on layer2 and 3

> 20MB/sec

–> satisfies our requirements

4. DAQ inefficiency



* deadtime ~ 10%@500Hz
* non−linear component
    <− found to be due to
    interference between
    2 DMAs

Other sources of inefficiency

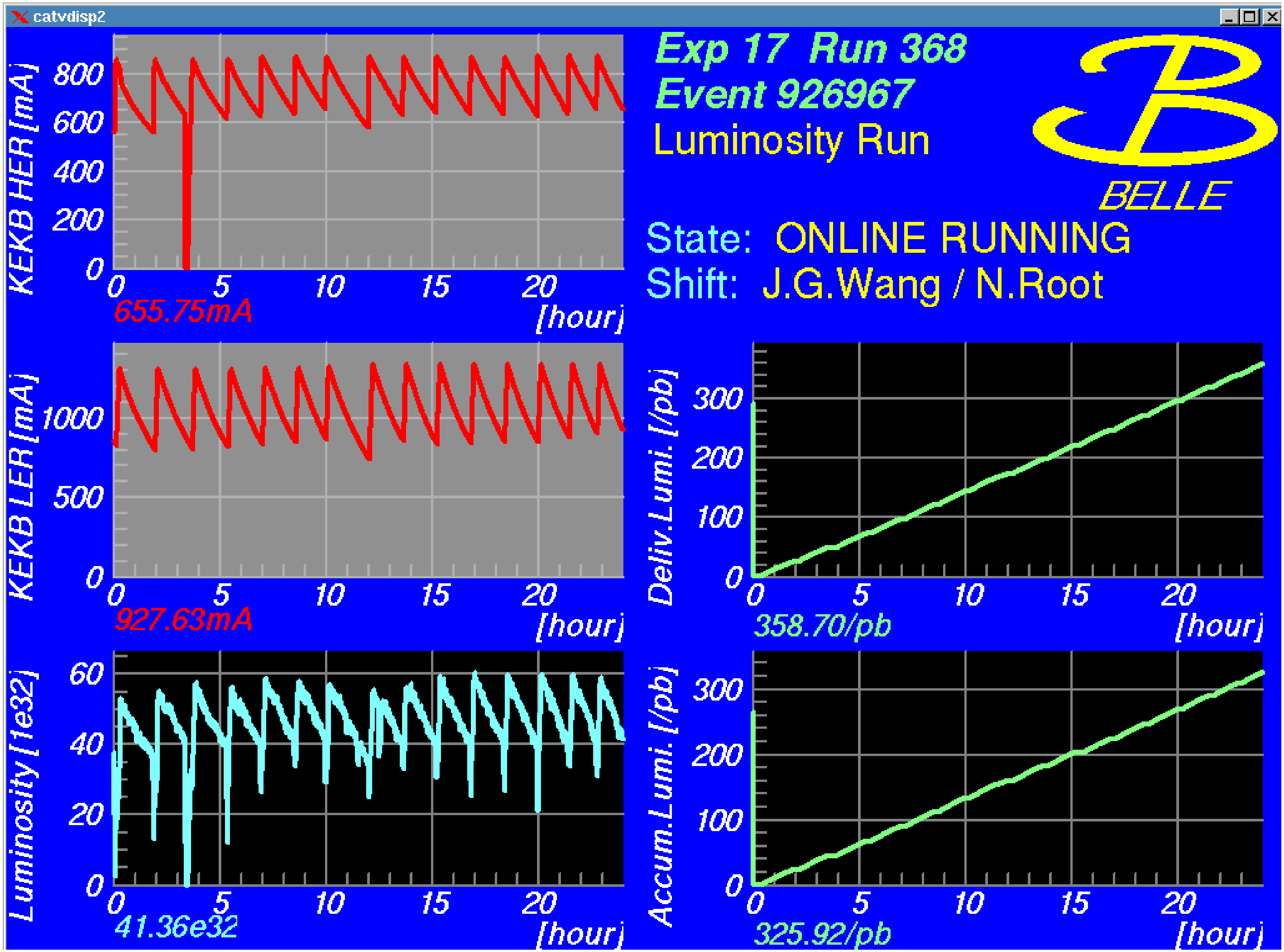
Typical patten of a run

- 1 run / 1 fill (topping)
- 1 run continues ~ 1 hour

1. Time to ramp up/down detector HV
   - ramp up time : ~ 1min
   - ramp down time : ~ 1min
2. Time to start/stop DAQ – run is started/stoped for every fill
   - ~ 30sec.
   - included in HV ramp up/down time
3. CDC current limitter : ~a few %
4. Various troubles : ~ a few %

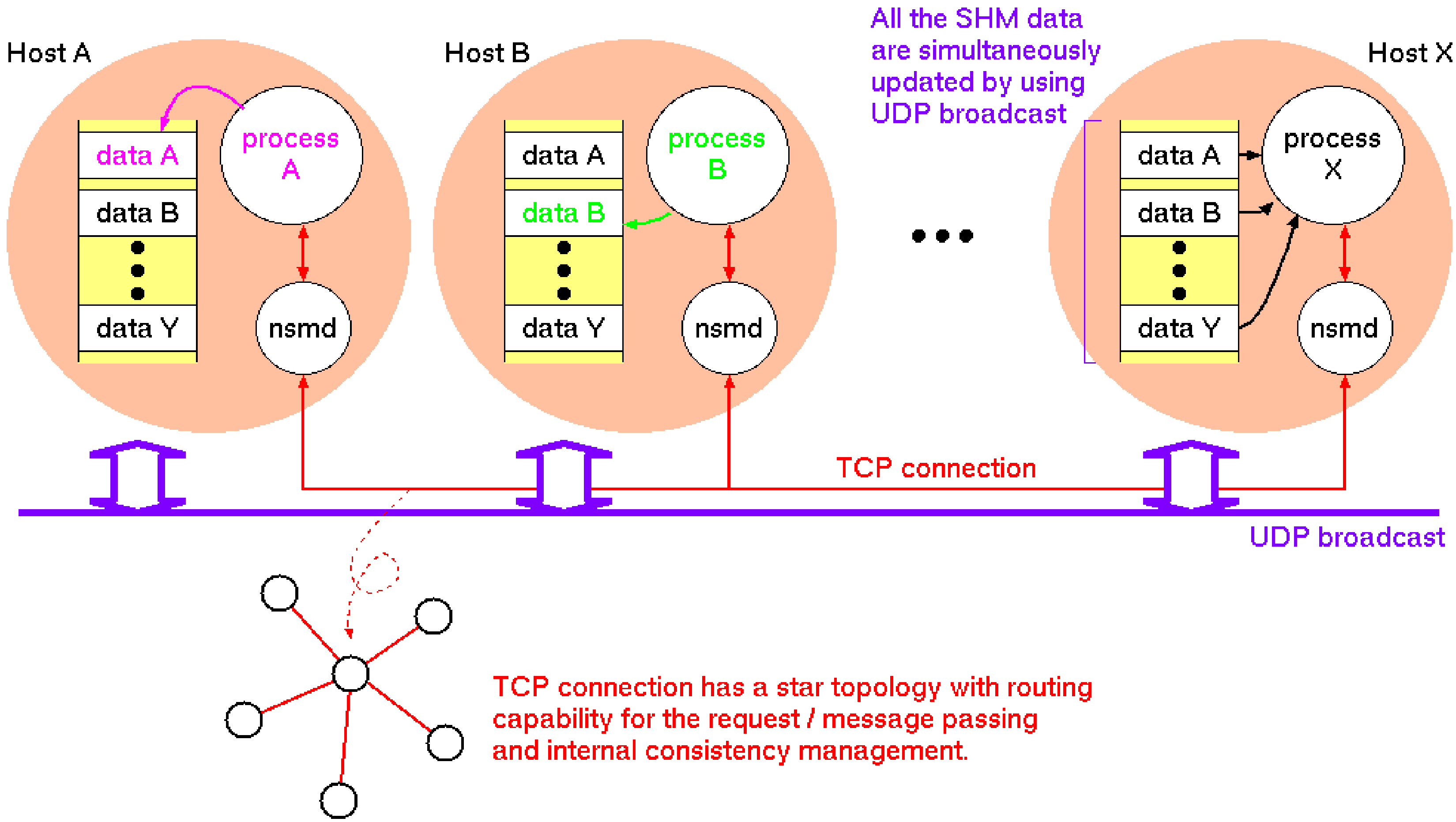
(5. Injection deadtime (2ms) in cotinuous injection : 1–2%)

Overall efficiency to delivered luminosity : ~ 90% (average)

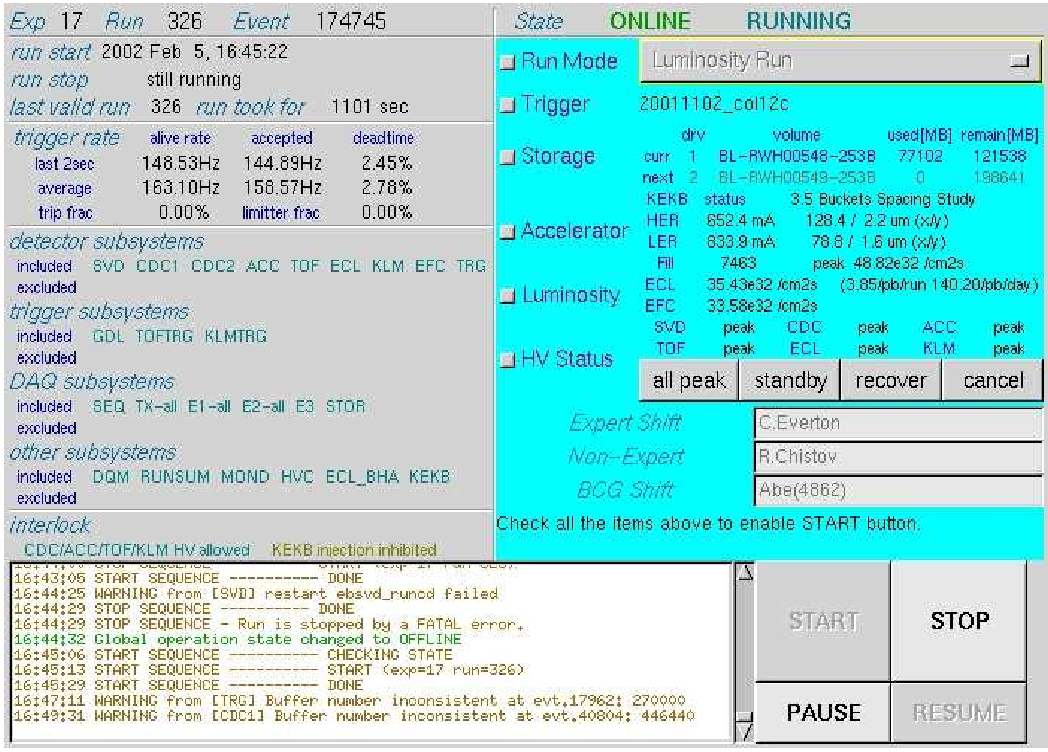

catvdisp2
Exp 17 Run 368
Event 926967
Luminosity Run
BELLE
State: ONLINE RUNNING
Shift: J.G.Wang / N.Root
KEKB HER [mA]
655.75mA
KEKB LER [mA]
927.63mA
Luminosity [1e32]
41.36e32
Deliv.Lumi. [/pb]
358.70/pb
Accum.Lumi. [/pb]
325.92/pb
[hour]

6. Run Control and Data Monitoring

Run Control

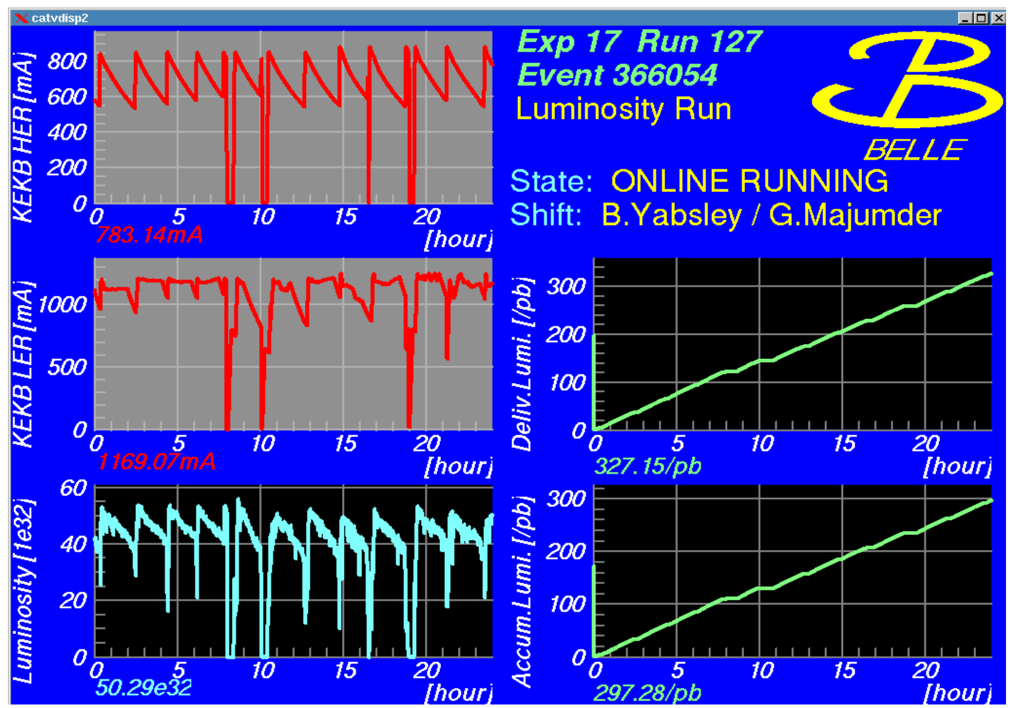


– Based on "NSM" : network shared memory
  * message passing between nodes
  * shared memory capability among distributed nodes

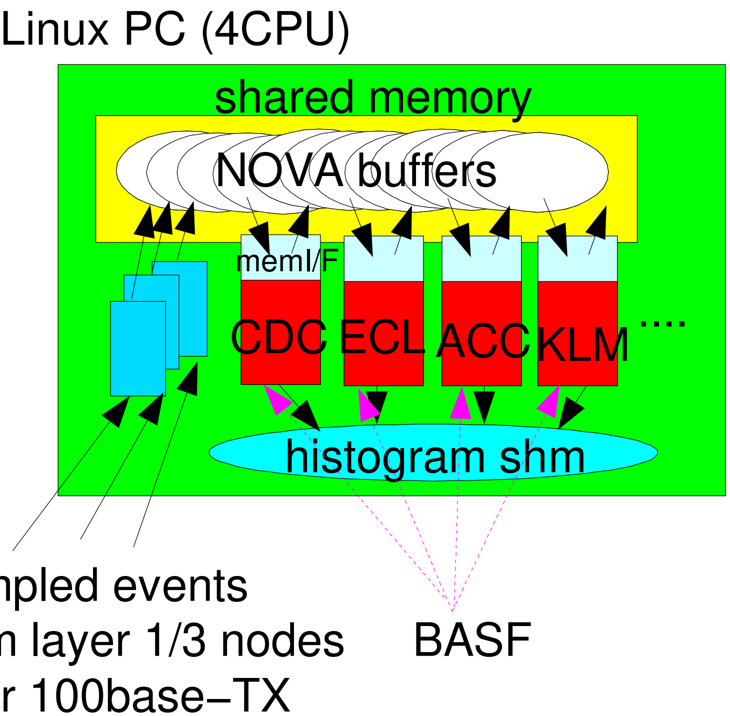


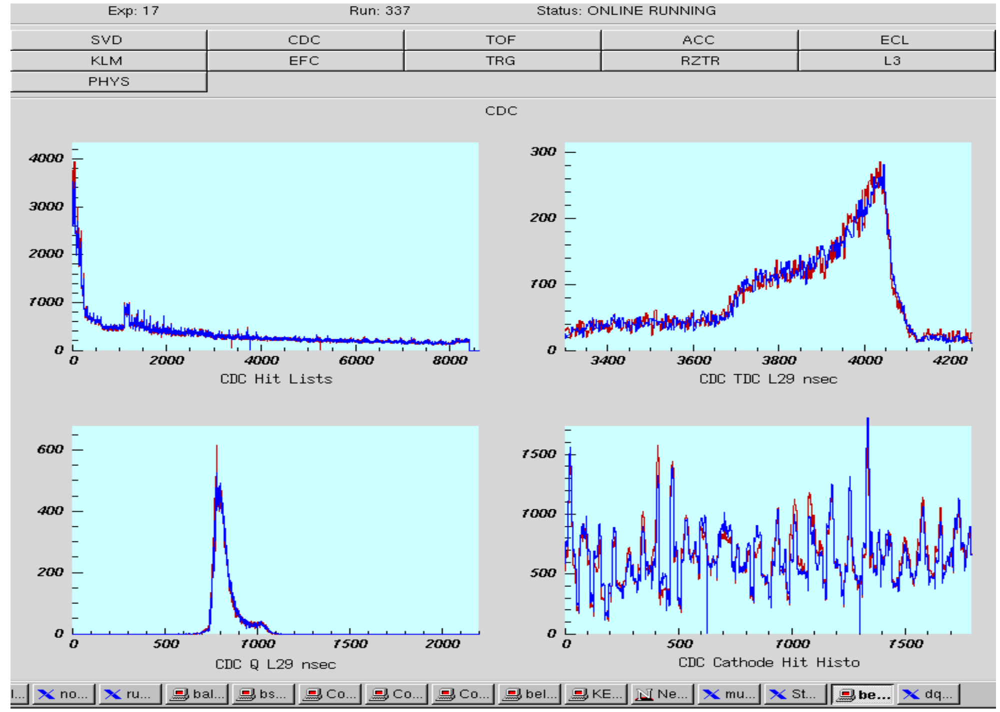
Run control panel

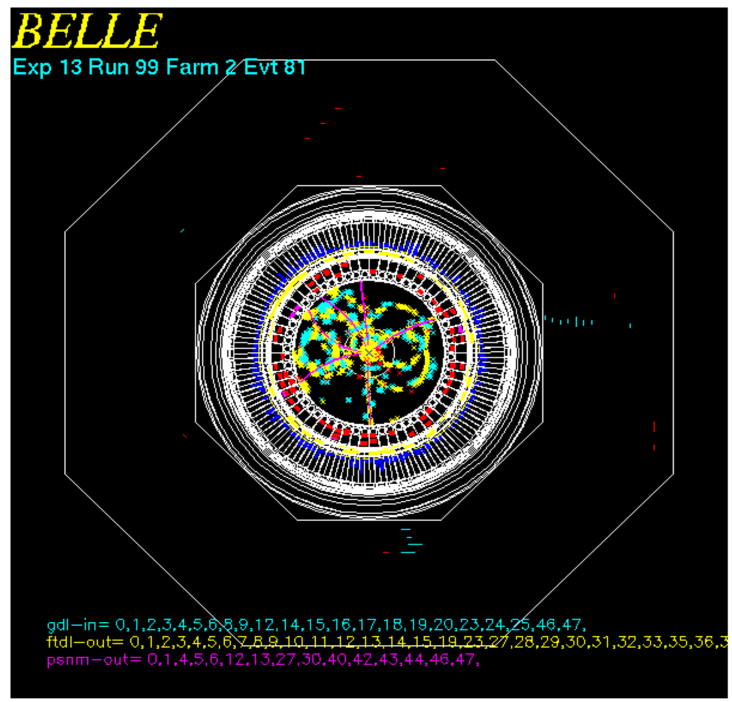
One day history panel



Data Quality Monitor







* Sampled events are queued in NOVA buffers and picked up by monitor programs running independently.
* Event display is also implemented as one of monitor programs.

5. Plan for upgrade

– Luminosity : still a half of design luminosity
  –> trigger rate is expected to increase by a factor of 2 or more

– SVD upgrade is planned next summer
  * beam pipe with smaller radius
  * new Z trigger may not work

Possibility of trigger rate increase up to 1KHz or more

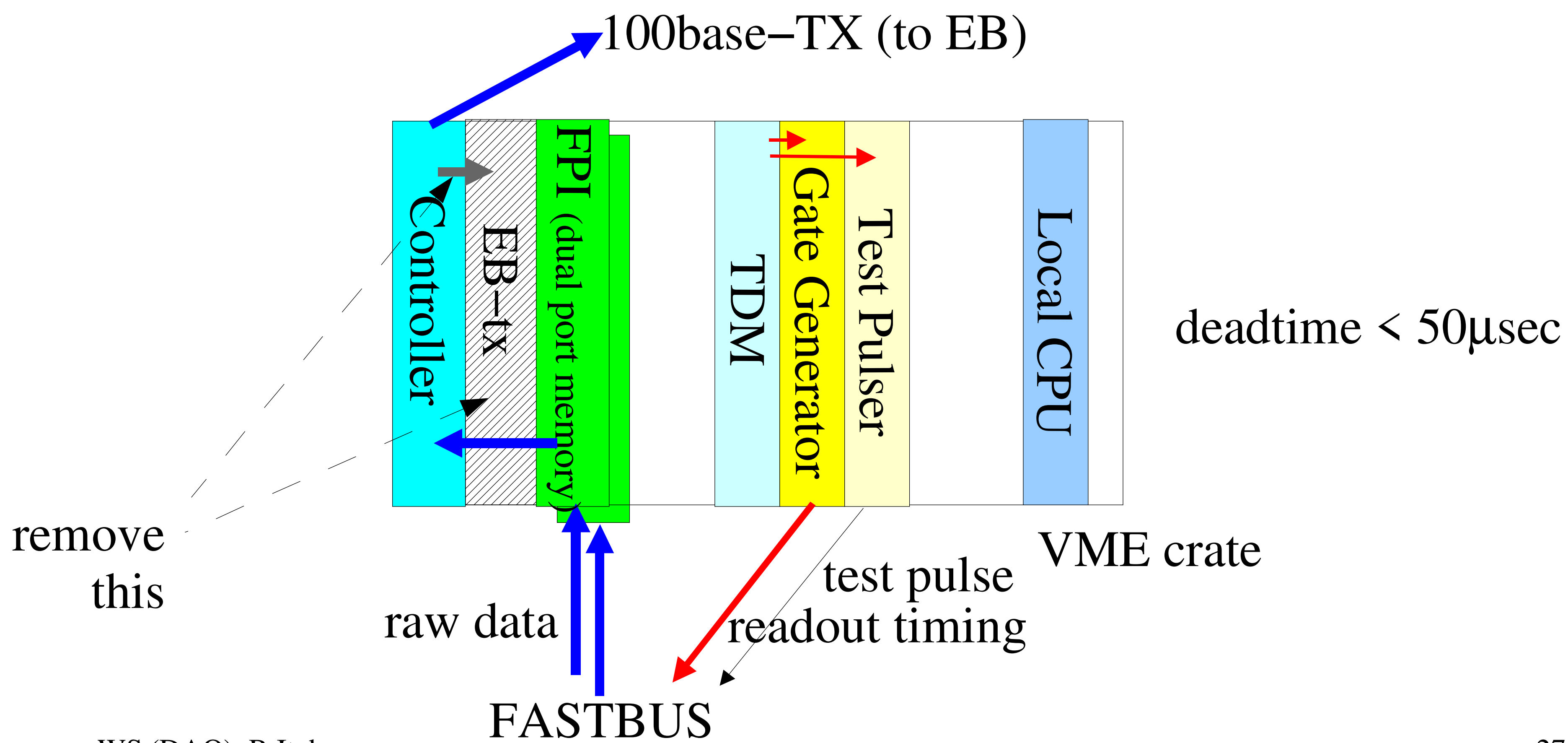
DAQ deadtime : 10% at 500Hz –> 20% or more

Need to reduce dead time to ~50μs level (~ 5% at 1KHz)
- SVD readout deadtime
- FASTBUS readout deadtime

a) FASTBUS subsystem

– Subdivision of readout subsystems
  8 readout subsystems –> 16

– Direct data transfer from FASTBUS to 100Base–TX (no 2–fold DMA)
  –> merge readout controller and EB–Tx functions into single
  VME processor board (MVME5100)



b) SVD readout

- HALNY/VME –> replaced with PC based readout subsystems by SVD upgrade
- Direct network connection (100base−TX or GbE) to event building farm
- Subdivision of readout subsystems : 4 –> 32

= PCI based FADC/DSP board is being developed.
expected readout deadtime : ~ 25μsec

c) Other improvements

- Reduction of time for starting/stopping DAQ
- Reduction of time for ramping up/down detector HV

Goal : > 95% efficiency at 1KHz

6. Summary

- The Belle Data Acquisition System is working fine under the current beam condition:
  Typical trigger rate ~ 250Hz; Event Size ~ 40KB
- Switchless event building scheme was developed and proven to work in the real experiment.
- The upgrade of DAQ is planned to cope with trigger rate of 1kHz or more expected after the upgrade of SVD.

SuperKEKB –> pipelined readout system required ... starting design