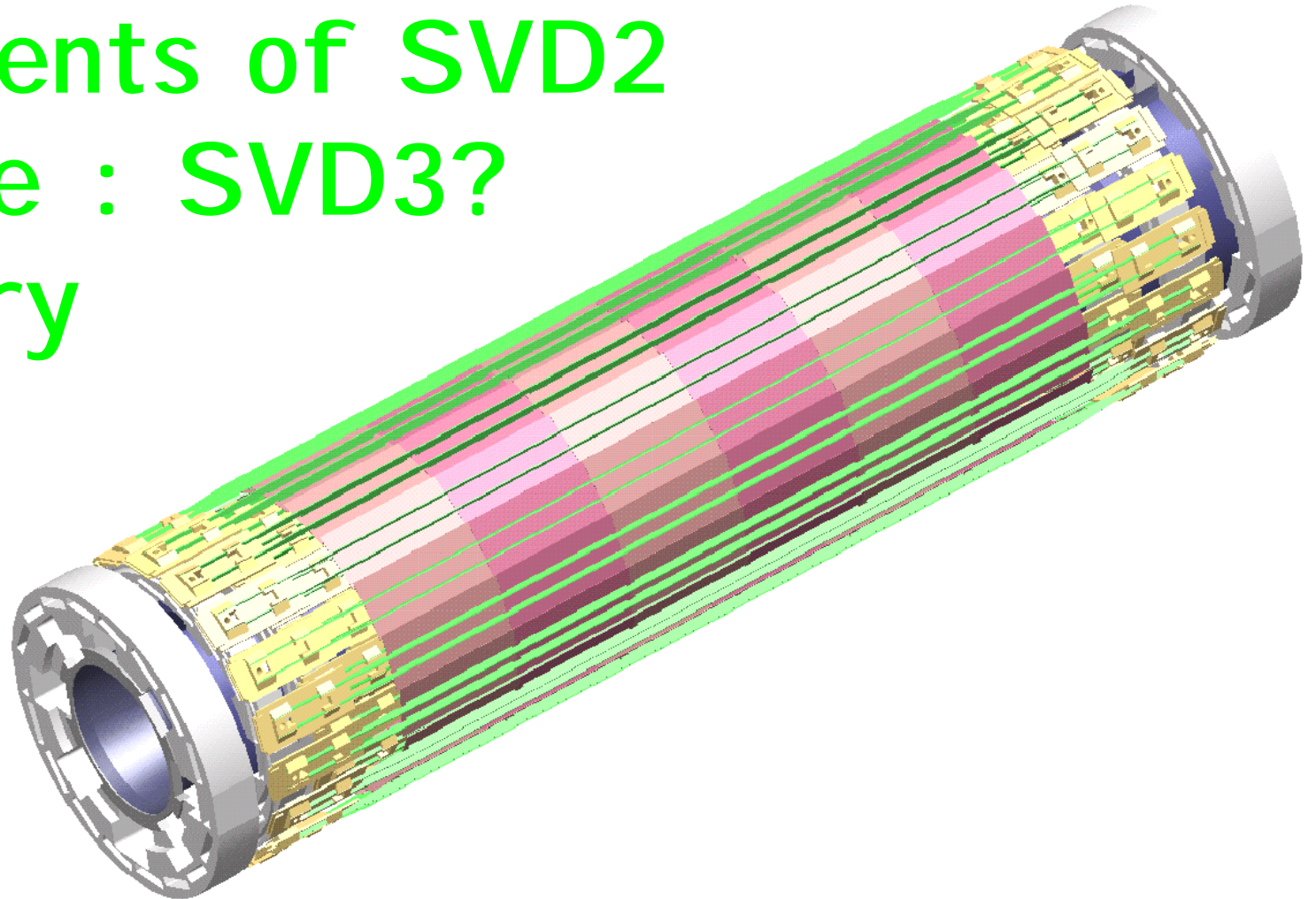


Belle Silicon Vertex Detector (II)

Y. Yamada (KEK) on Feb. 15, 2002

1. Introduction to SVD2
2. Components of SVD2
3. Upgrade : SVD3?
4. Summary



1. Introduction to SVD2

- Better impact parameter resolution
- Better tracking efficiency for slow π

$R_{bp}^{in} = 2.0$ cm

3 layers: $R = 3.0, 4.5, 6.0$ cm

8+10+14=32 ladders

SVD1

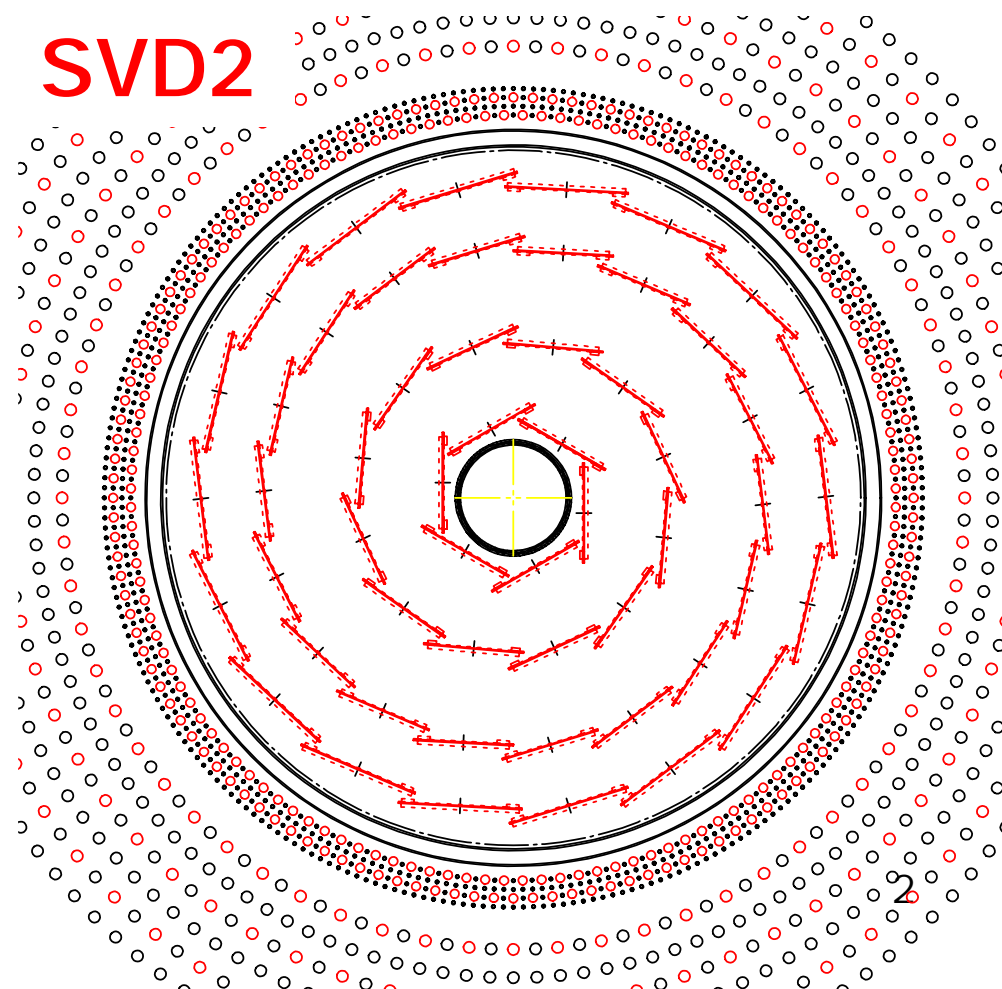
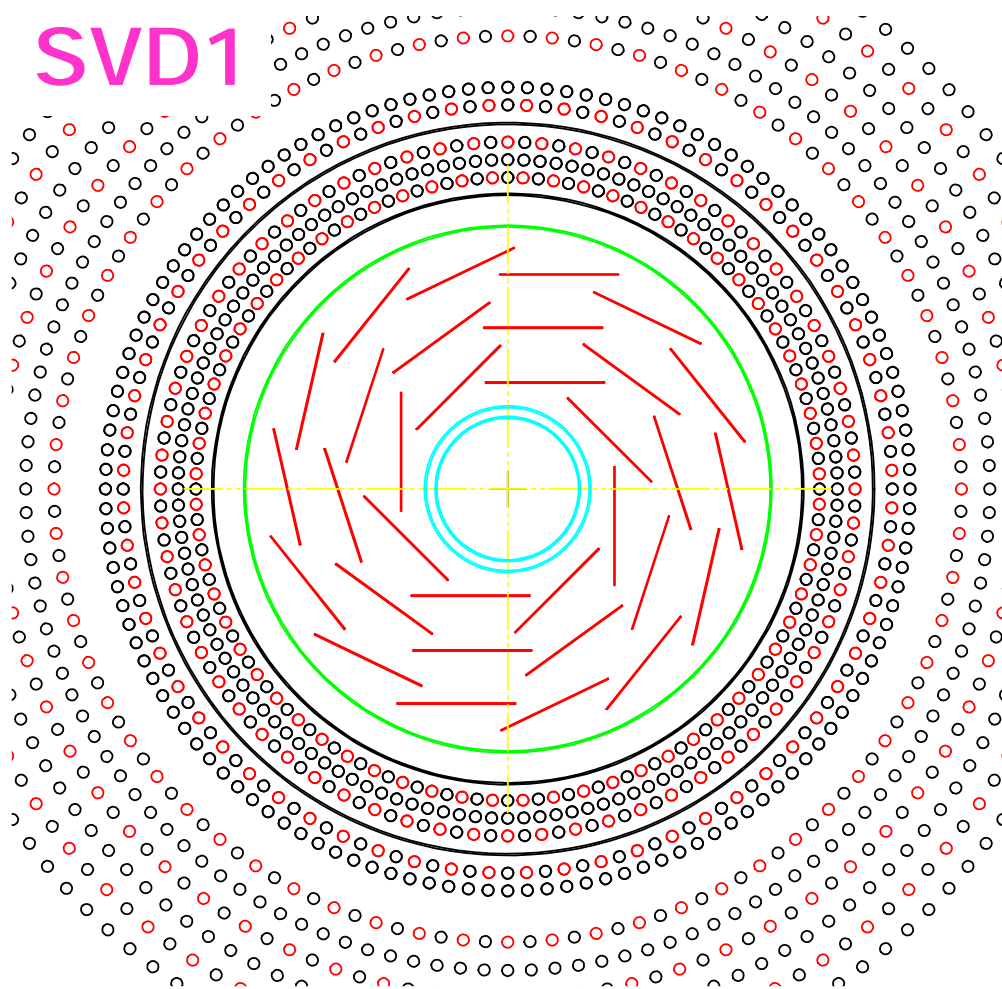


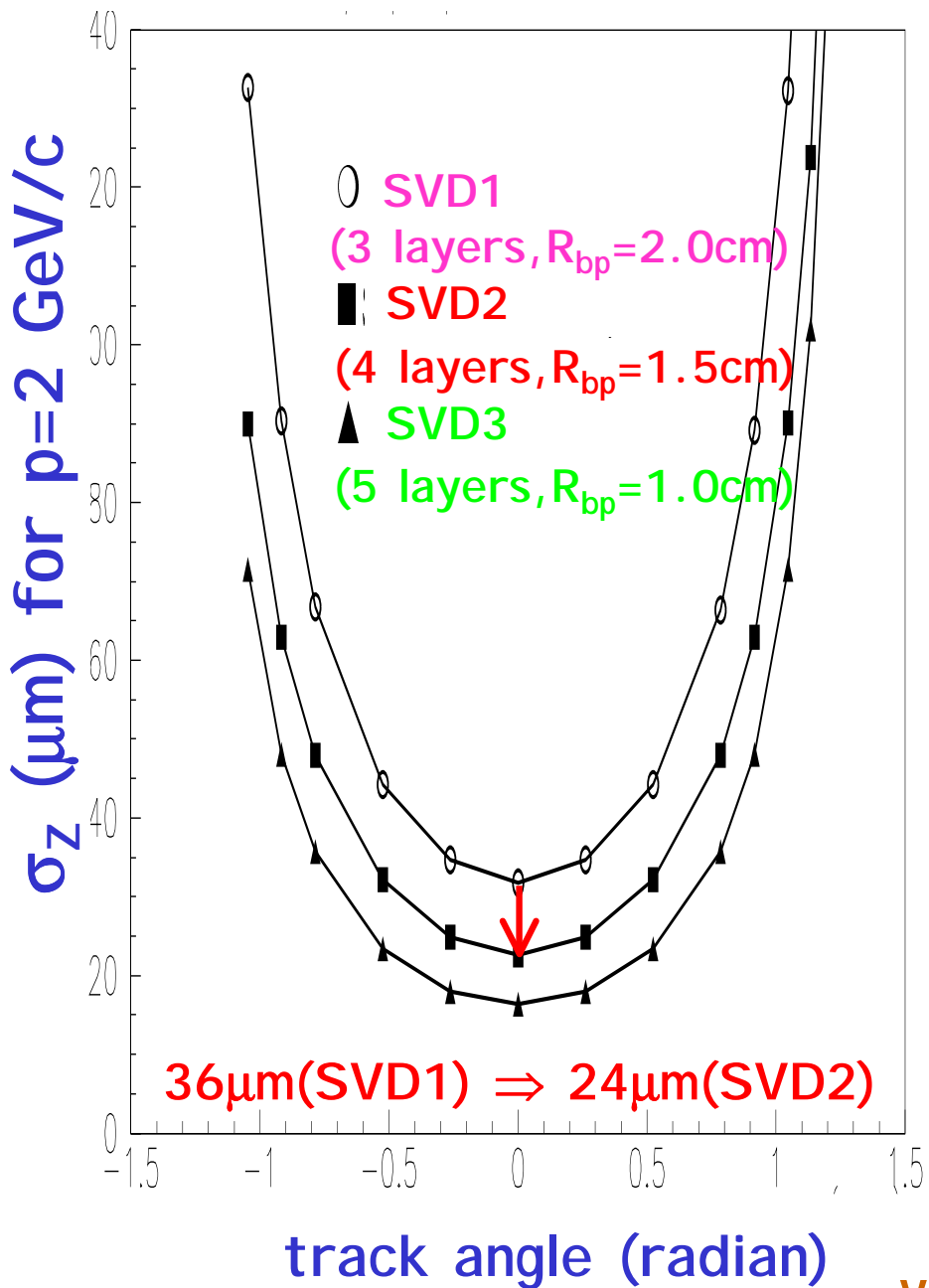
$R_{bp}^{in} = 1.5$ cm

4 layers: $R = 2.0, 4.4, 7.0, 8.8$ cm

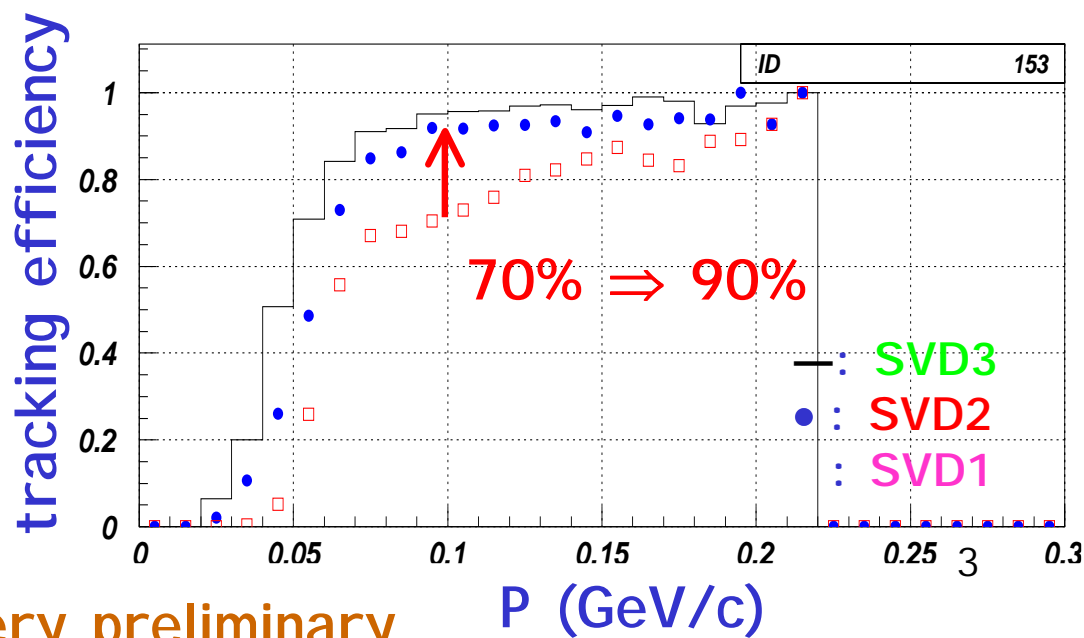
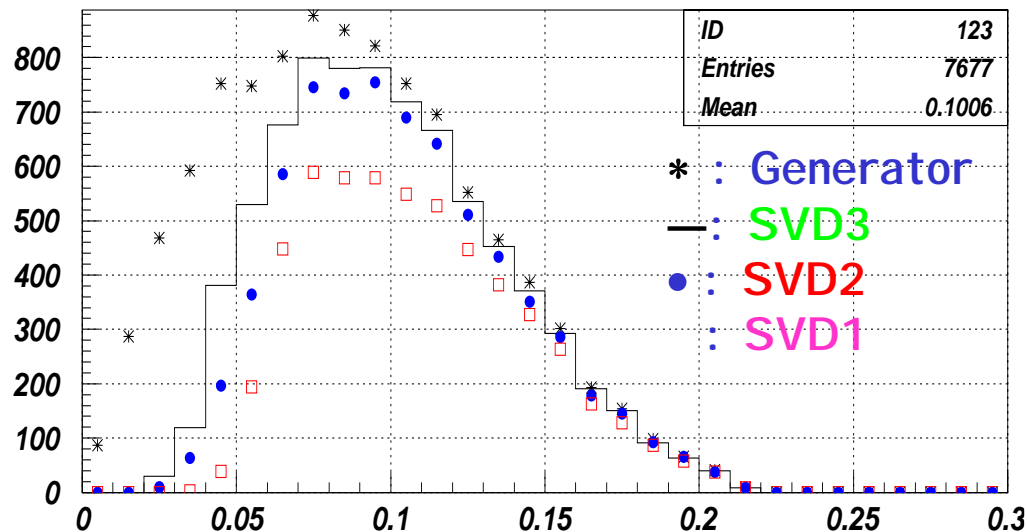
6+12+18+18=54 ladders

SVD2





momentum reconstruction for slow π in $B \rightarrow D^* l \nu$



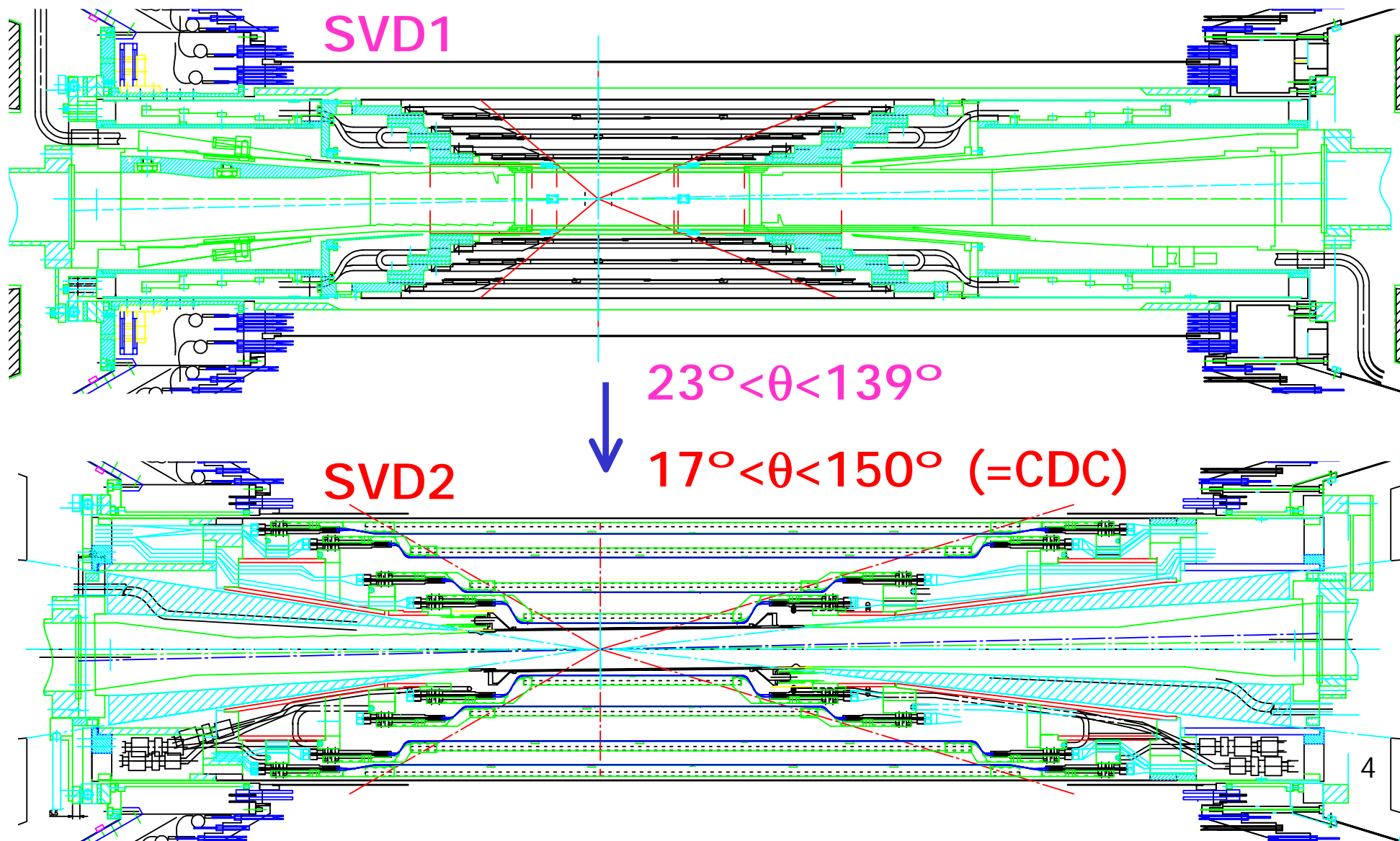
very preliminary

P (GeV/c)

Increase of acceptance

- Larger acceptance

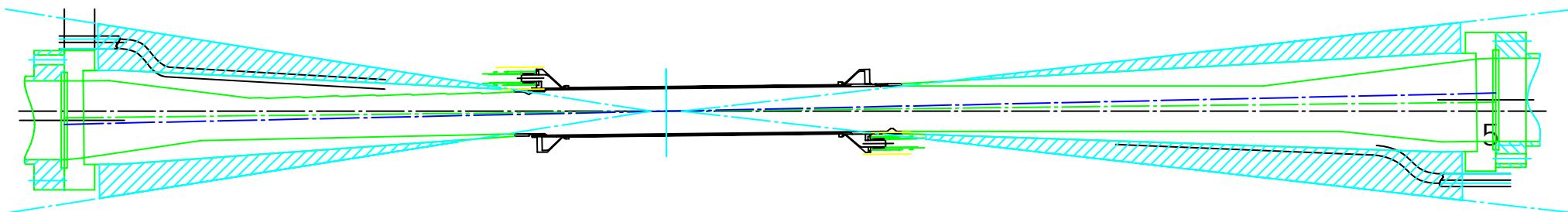
Outermost ladder : $L=22\text{cm}, R=6.0\text{cm} \Rightarrow L=46\text{cm}, R=8.8\text{cm}$



•Simulation study on beam background

	SVD1.4 $R_{bp}=2.0\text{cm}$ @ 0.6/0.8A	SVD1.4 $R_{bp}=2.0\text{cm}$ @ 1.1/2.6A	SVD2 $R_{bp}=1.5\text{cm}$ @ 1.1/2.6A	SVD3 $R_{bp}=1.0\text{cm}$ @ 1.1/2.6A
# of layers/ R_{1st}	3/3.0cm	3/3.0cm	4/2.0cm	5/1.5cm
SVD 1st layer dose(krad/yr= 10^7 s)	~40	~130	~80	~660
CDC 1st layer Occup.	$\equiv 1$	~3	~1.5	~3.6
SVD 1st layer Occup.	$\equiv 1$	~3	~ 0.9	~ 8
$\sigma_{\Delta Z}$ (μm)	~100	~100 \times 1.2?	~75	~50 \times 1.3?

- R_{inner} : 2.0cm \Rightarrow 1.5 cm
- Better cooling (He \Rightarrow PF200) for higher beam current
- More masks for charged particle background
- will be delivered in June by IHI

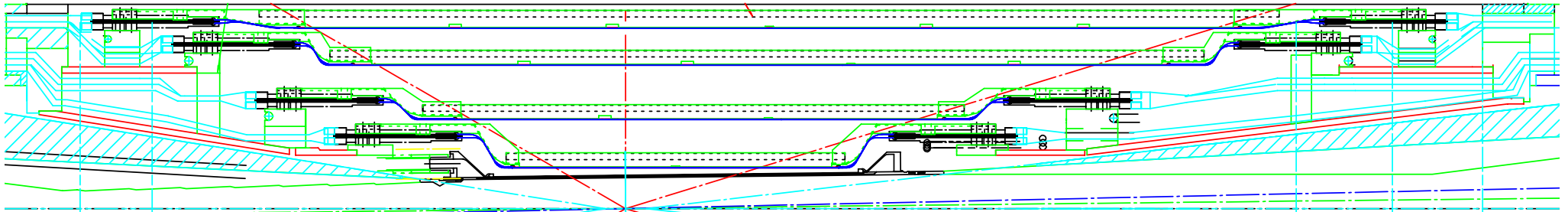
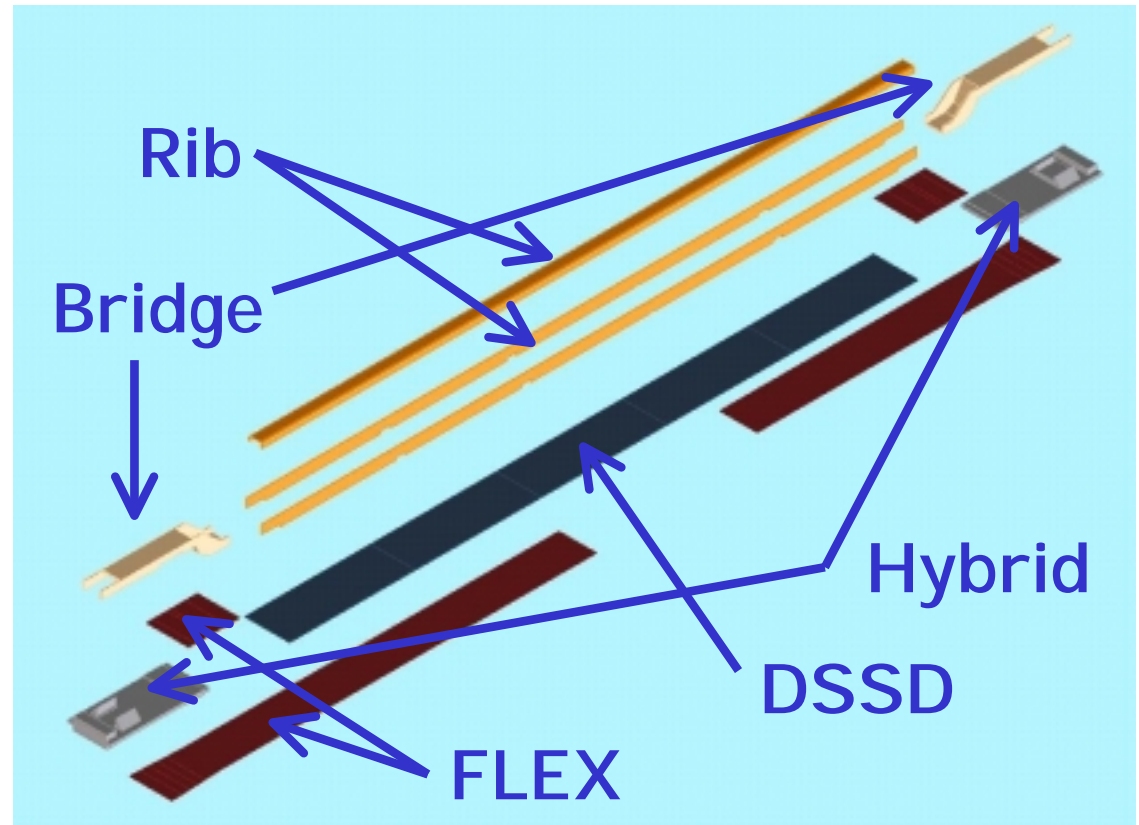


- New DSSD (CLEO3 type) : no pinhole problem
 - AC couple \Rightarrow DC operation
 - Double metal layer \Rightarrow FLEX readout
- More radiation hardness
 - VA1-0.8 μ m : 1 MRad \Rightarrow VA1-0.35 μ m : >20 MRad
- Better trigger capability
 - VA1 \rightarrow VA1TA (VA1 with trigger)
 - Introduction of Level-1.5 trigger in SVD FADC system
 - Introduction of small cell chamber
 - Faster SVD / CDC_{smallcell} electronics
 - \Rightarrow trigger rate @ design current : 1400 Hz \rightarrow 500? Hz

DSSD ladder

4 kinds of half ladders

L	Backward	forward
1	1-DSSD	1-DSSD
2	2-DSSD	1-DSSD
3	3-DSSD	2-DSSD
4	3-DSSD(W)	3-DSSD(W)



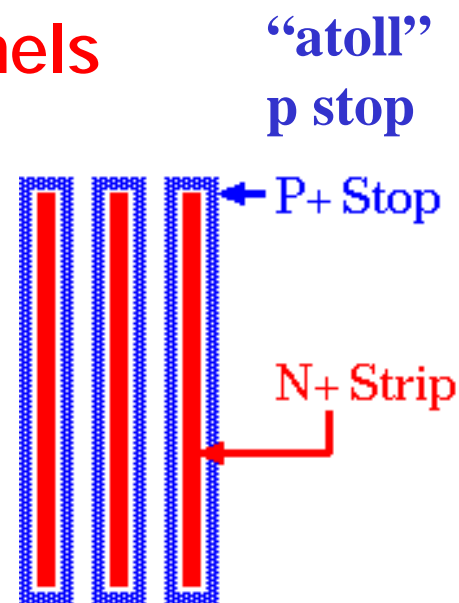
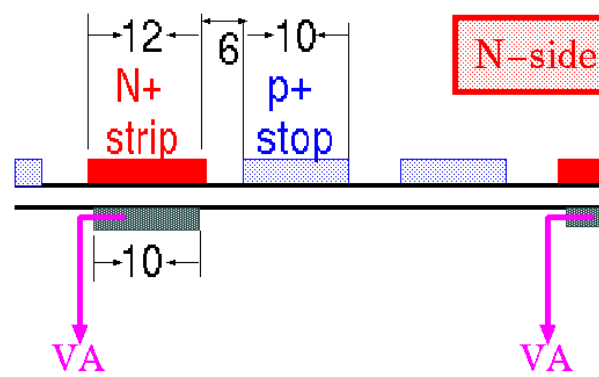
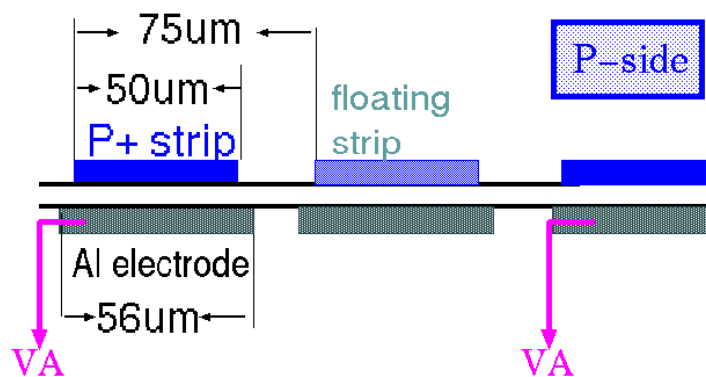
- Prototyping and electrical test of the half ladder finished.
- Mass production will start soon in Melbourne and HPK.

DSSD (DSSD4387 manufactured by HPK for Belle)

- AC couple, but DC readout by floating ground
- already delivered

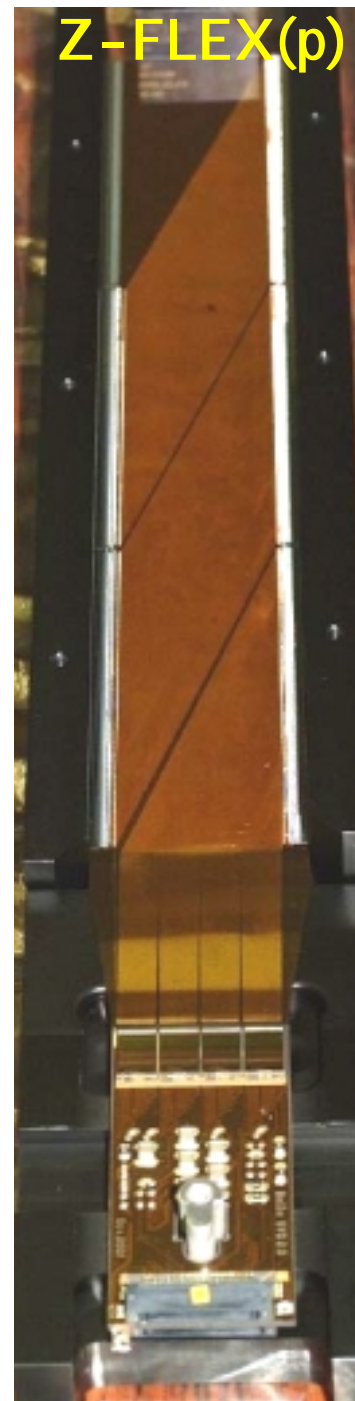
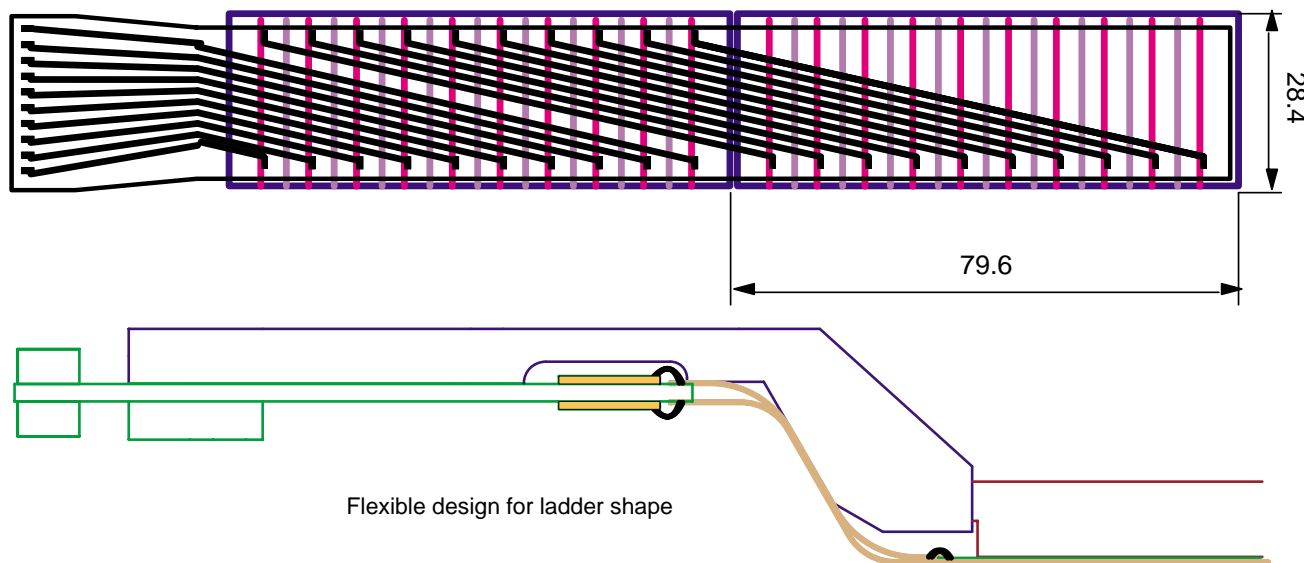
	p-side (Z)	n-side ($r\phi$)
Active area (mm ²)	76.8 × 25.6	76.8 × 25.6
(4 th layer)	(73.8 × 33.3)	(73.8 × 33.3)
Strip pitch (μm)	75 (73)	50 (65)
Readout pitch (μm)	150 (Cap. charge div.)	50
# of readout	512	512
Bias (volt)	-5	+70

• 512x2(p/n)X2(F/B)X54(ladders)=110,592 channels



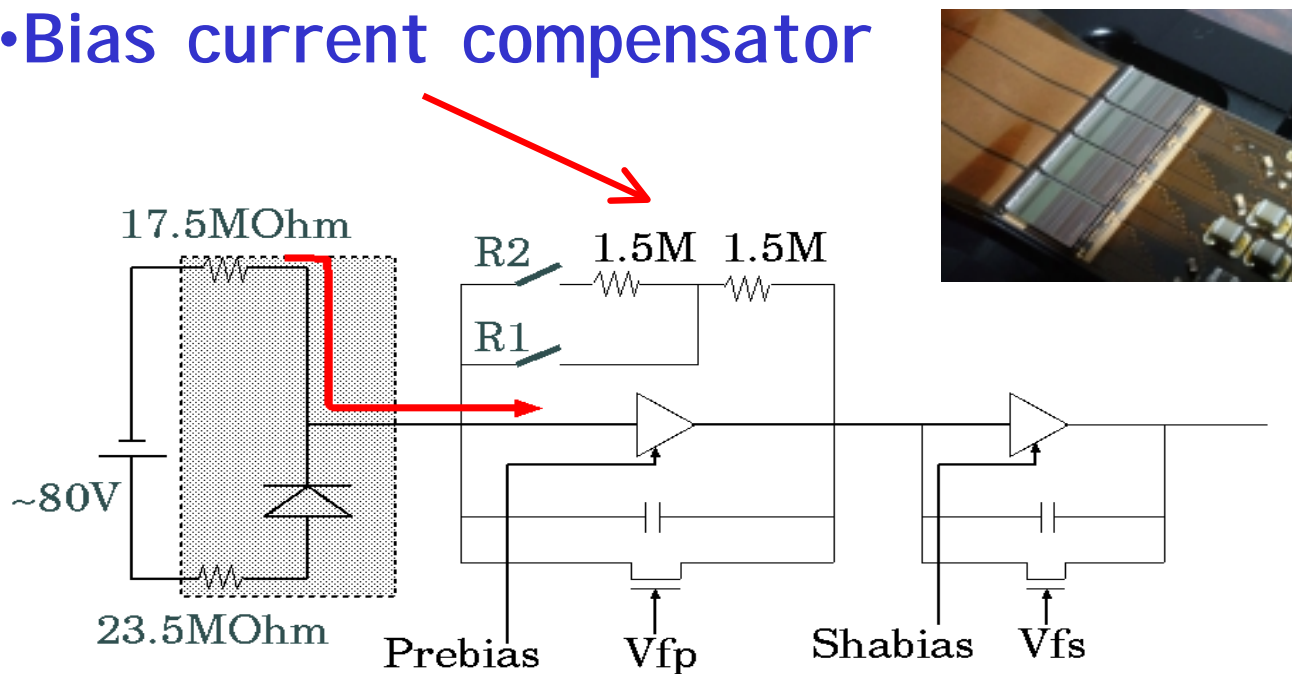
FLEX circuit

- Flexible layout of Si detector
- Lower capacitance than double metal
- Fine pitch ($\sim 50\mu\text{m}$)
- Wide area ($\sim 30 \times 3.3\text{cm}^2$)
- Under mass production
- Yield is issue for 3-DSSD

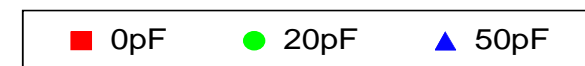
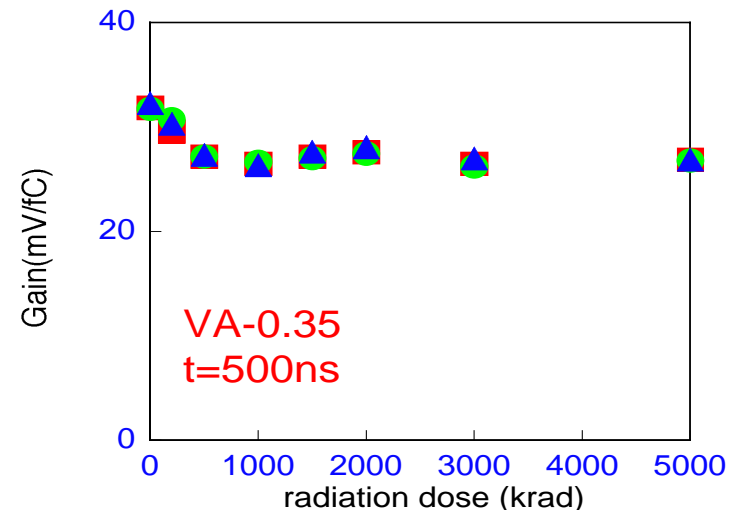


VA1TA

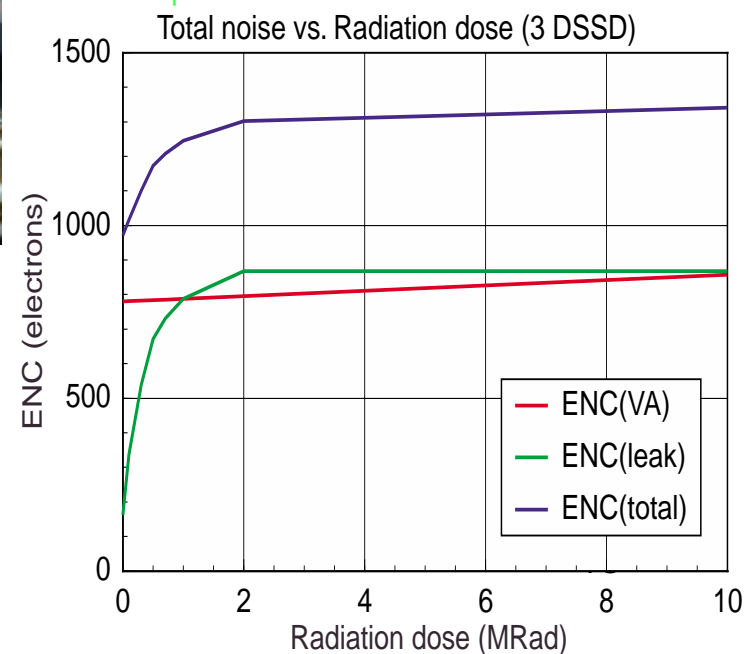
- VA1 (AMS-0.35 μm , $\tau_p=0.3\sim 1.0\mu\text{s}$)
+ TA (fast shaper and discriminator)
- Radiation hardness up to >20 MRad
- ENC ~ 800(e), S/N ~ 25
- four VA1TAs on a hybrid
- four analog signals read out in parallel
- Bias current compensator



Gain vs. rad. dose

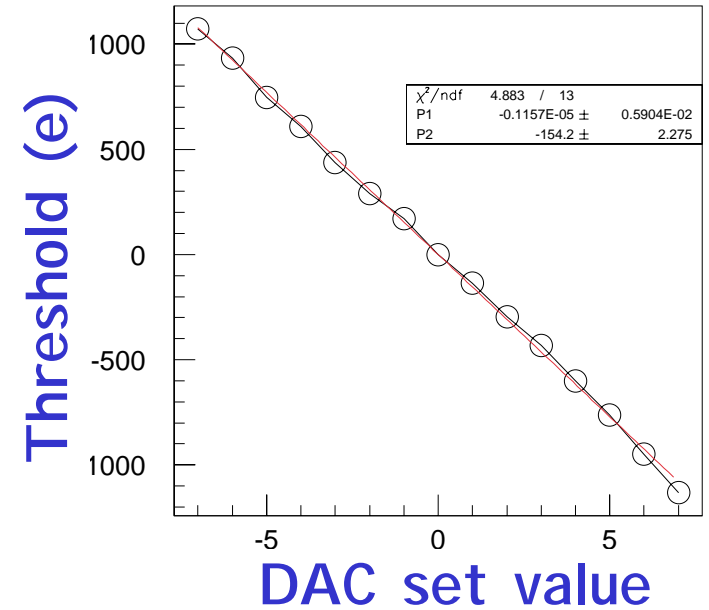
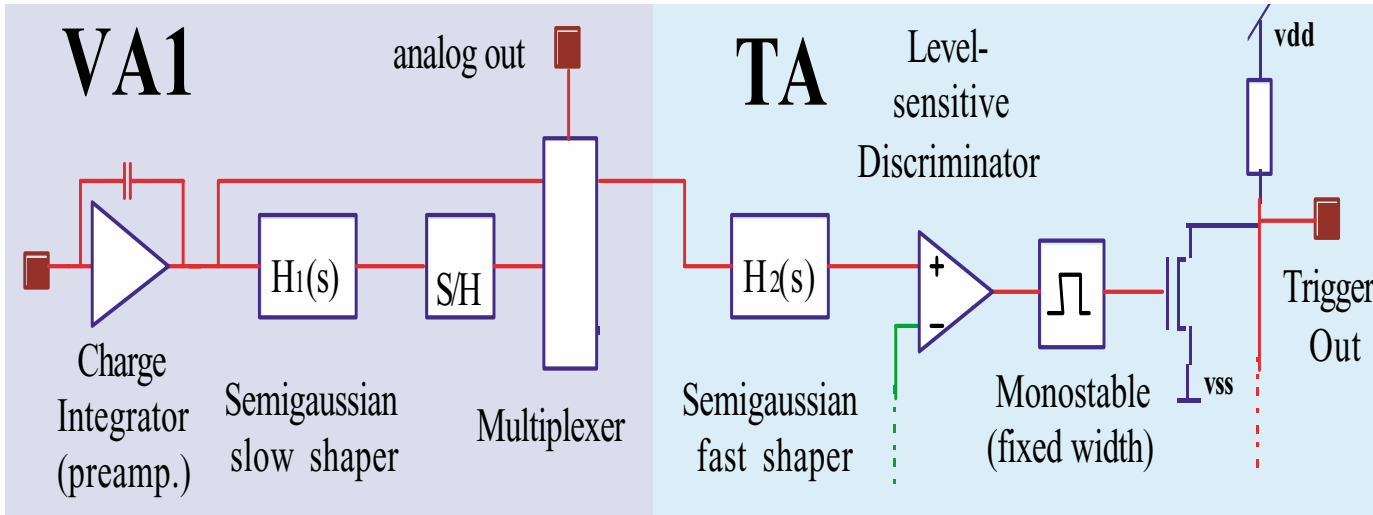


Expected noise for 3 DSSD ladder

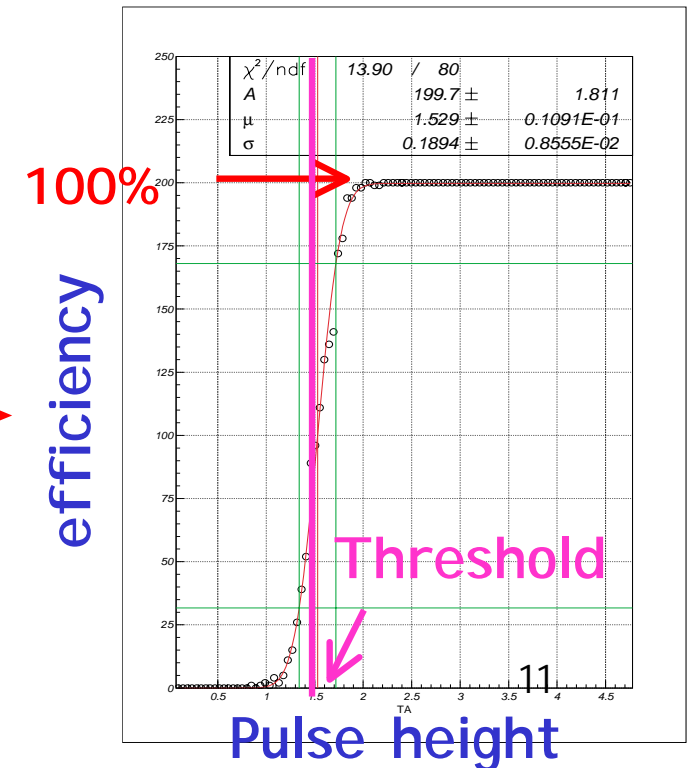
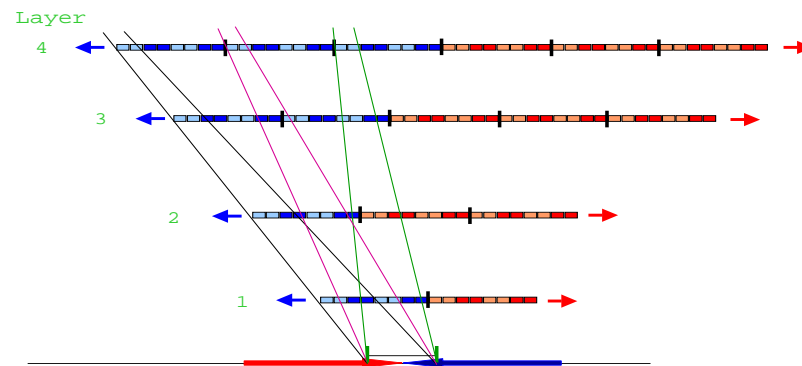


VA1TA (cont.)

- Trigger function was confirmed
- 128 channels/chip, 4 mW/channel
- Hybrid board under mass production

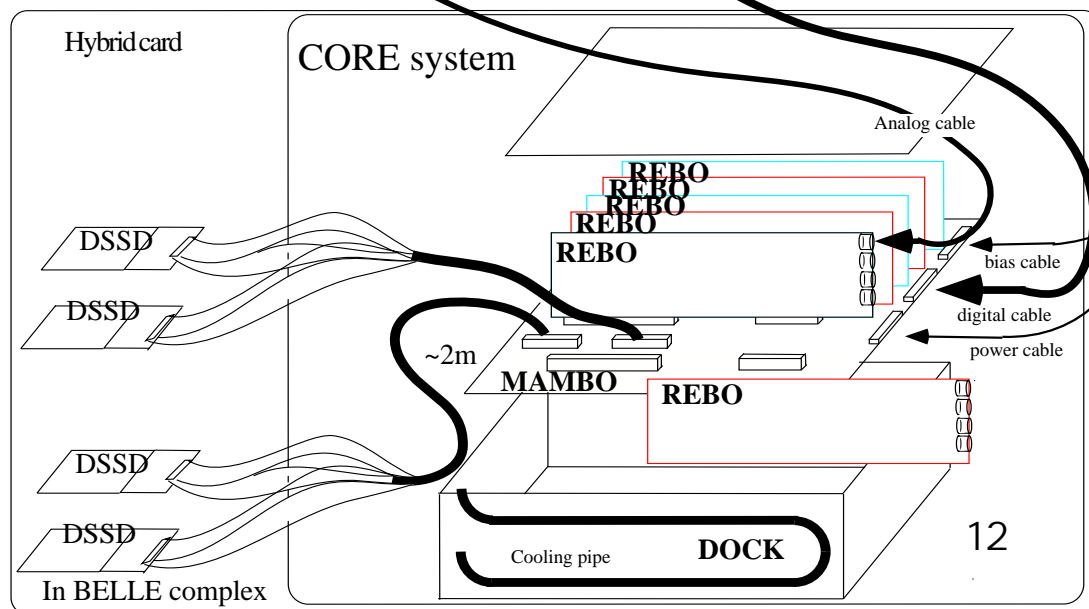
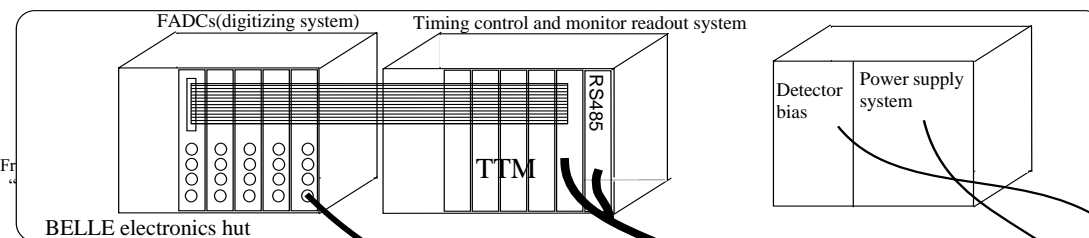
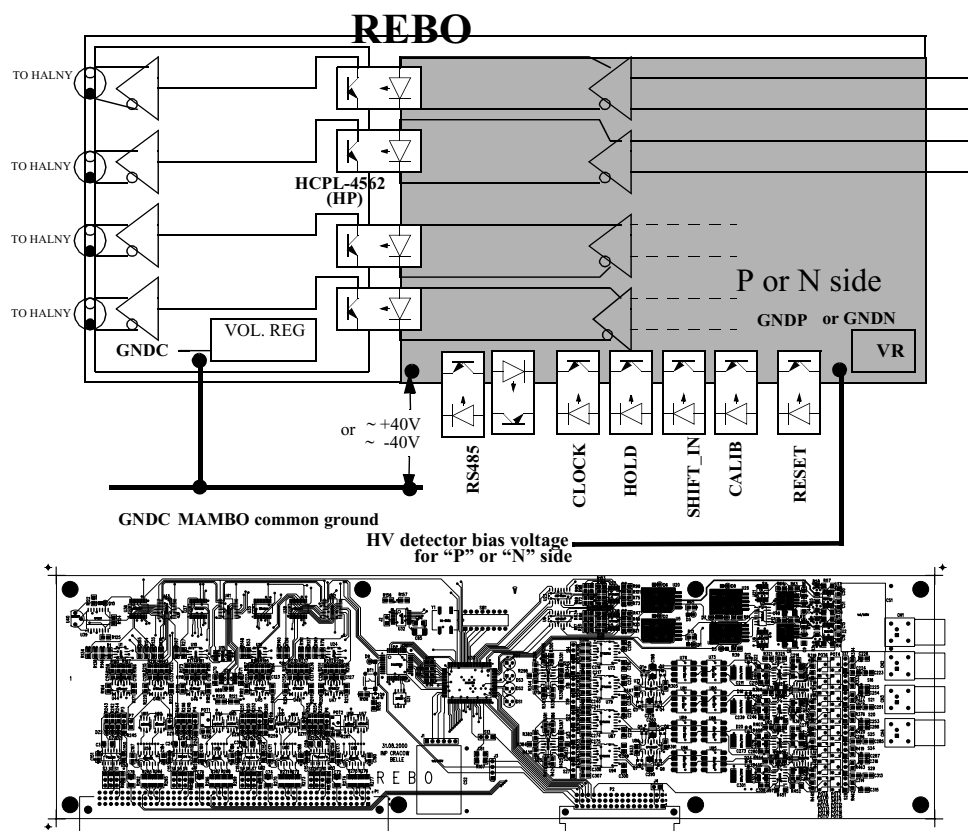


- Level-0 trigger logic in FADC are under study



Repeater system for SVD2 (3)

- Two floating grounds for p/n side
- one ground in one repeater board (REBO)
- 3-REBO(p-side)+3-REBO(n-side) on a board (MAMBO)
- 16 signals (from 4 hybrids) read by one REBO
- Optical couplers for analog/digital signals
- Prototype is under test



New FADC system

- 24 FADC(40MHz, 10 bit) on a board
- search L-0 triggers (VA1TA, TOF)
- generate L-1.5 trigger signal
- two events data can be stored
- prototype finished

Backend electronics schematic diagram

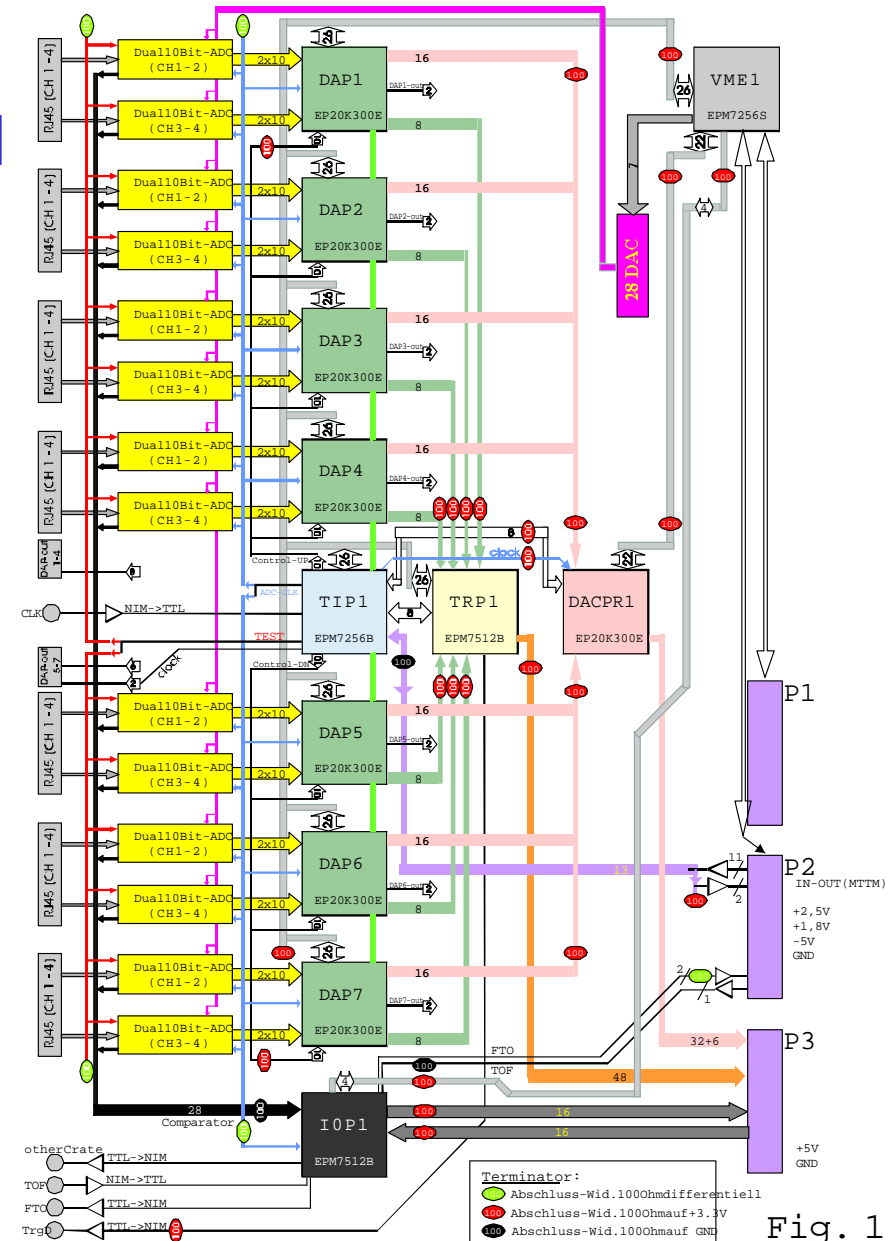
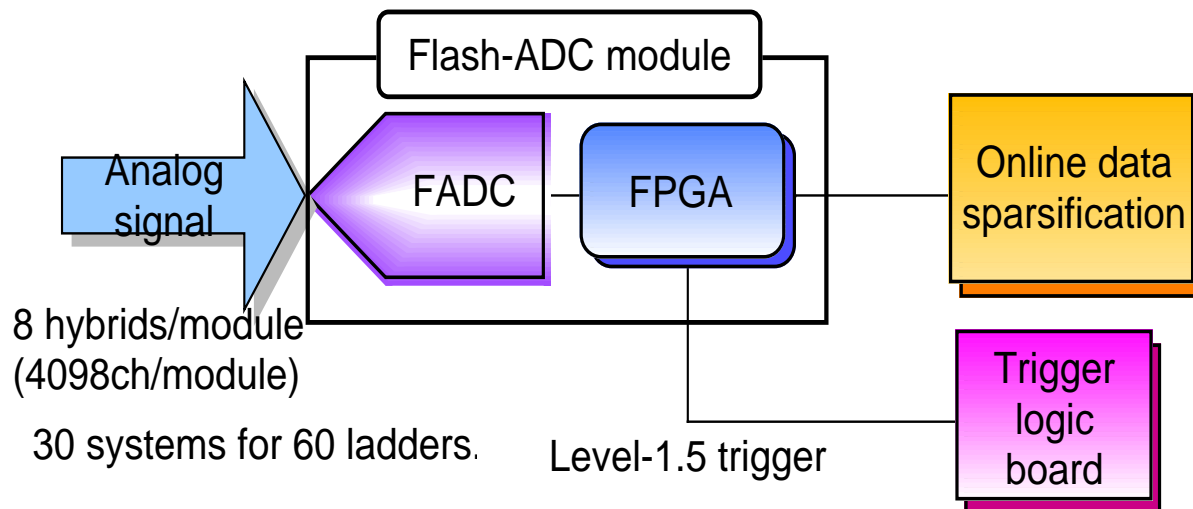
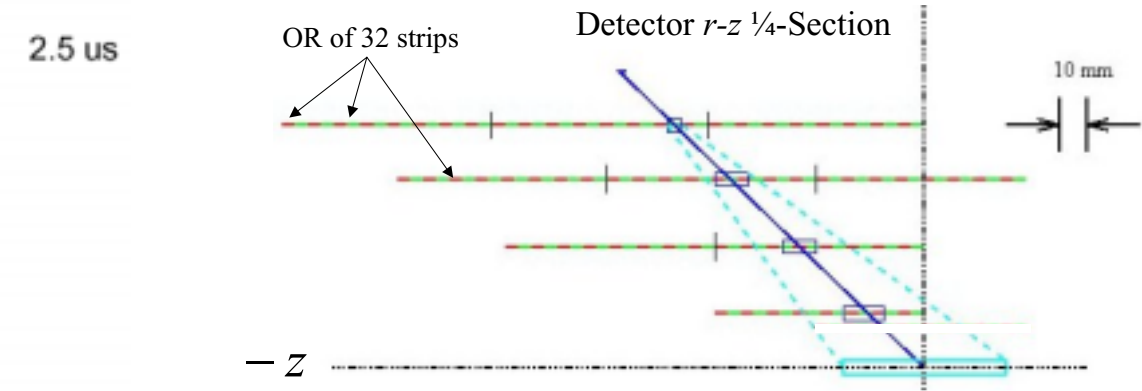
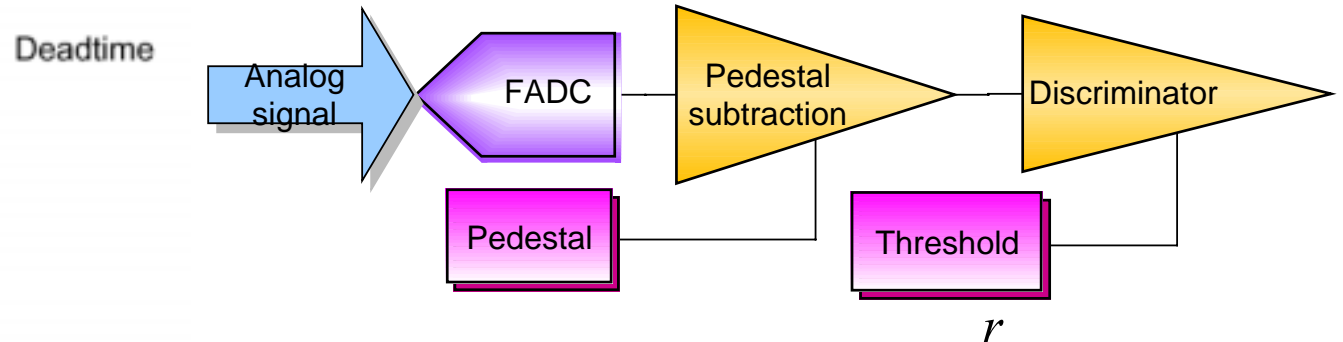
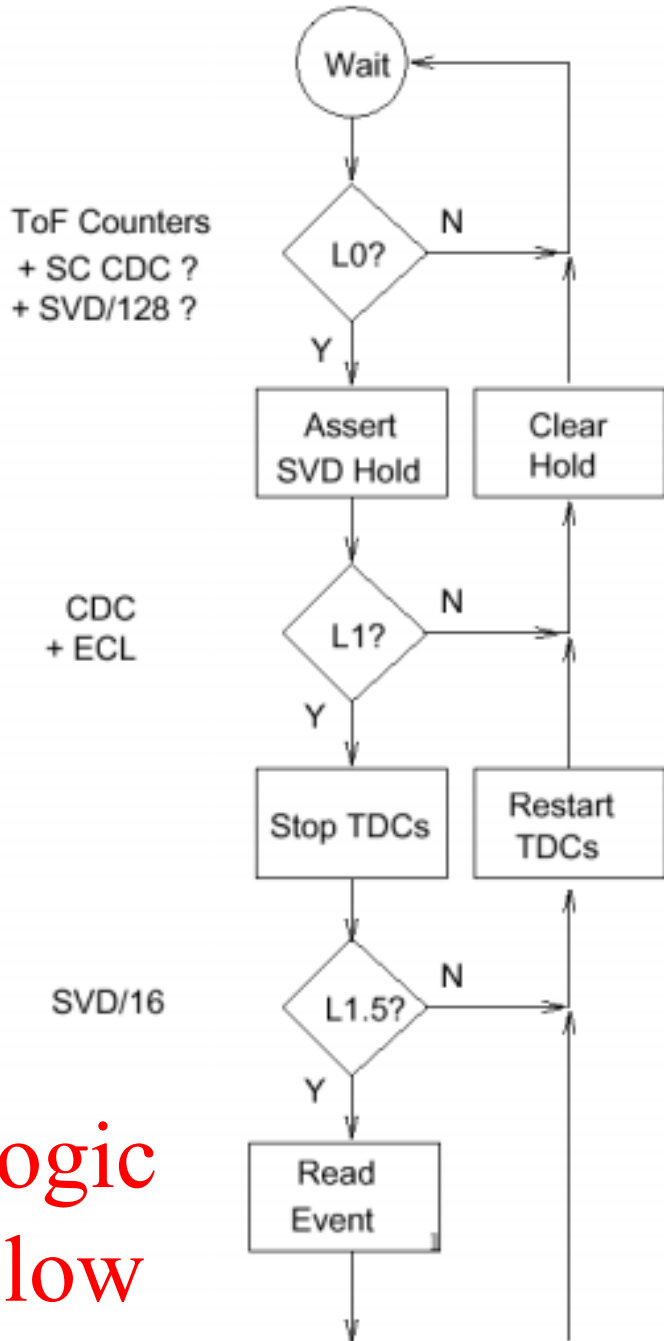


Fig. 1

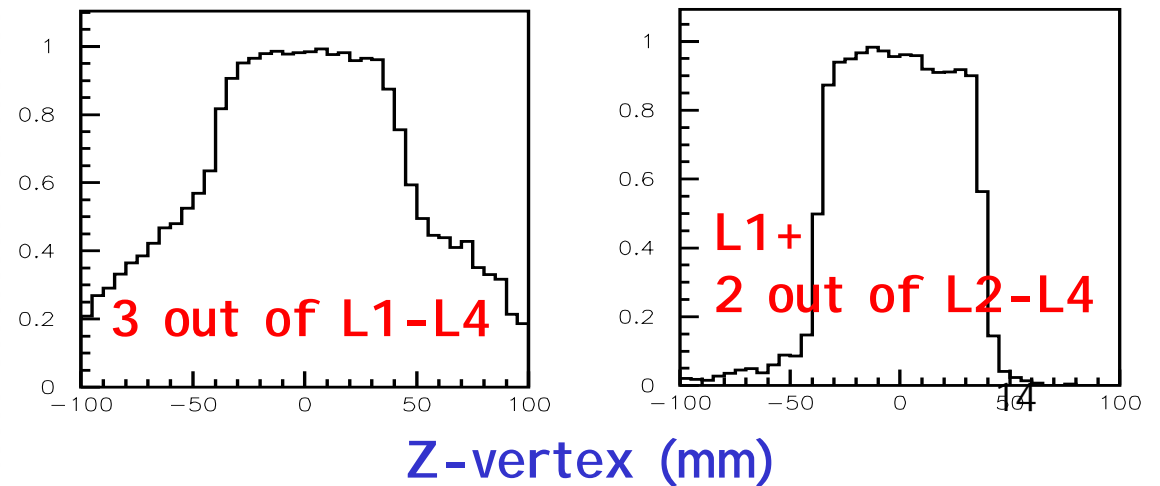
Level 1.5 trigger for SVD2

FPGA algorithm for L1.5 trigger



25 us

L-1.5 trigger efficiency (MC)

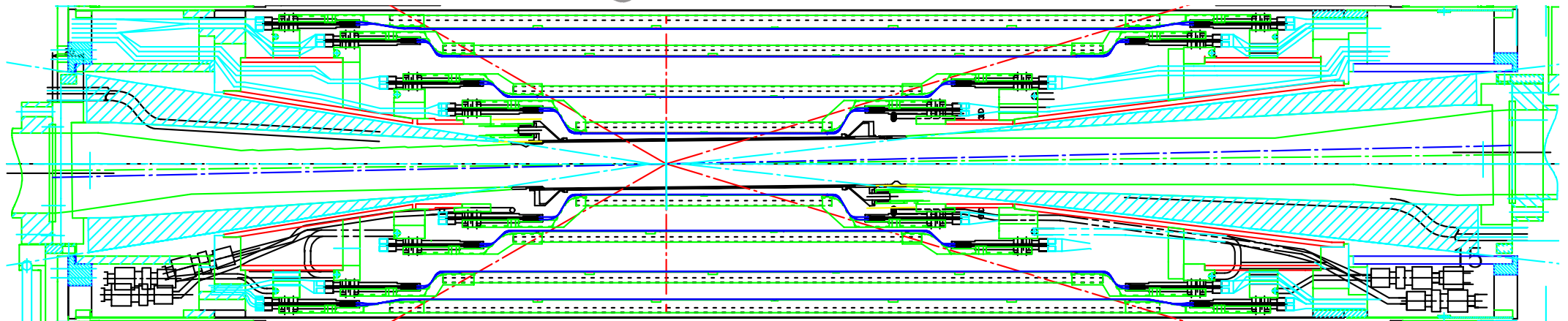
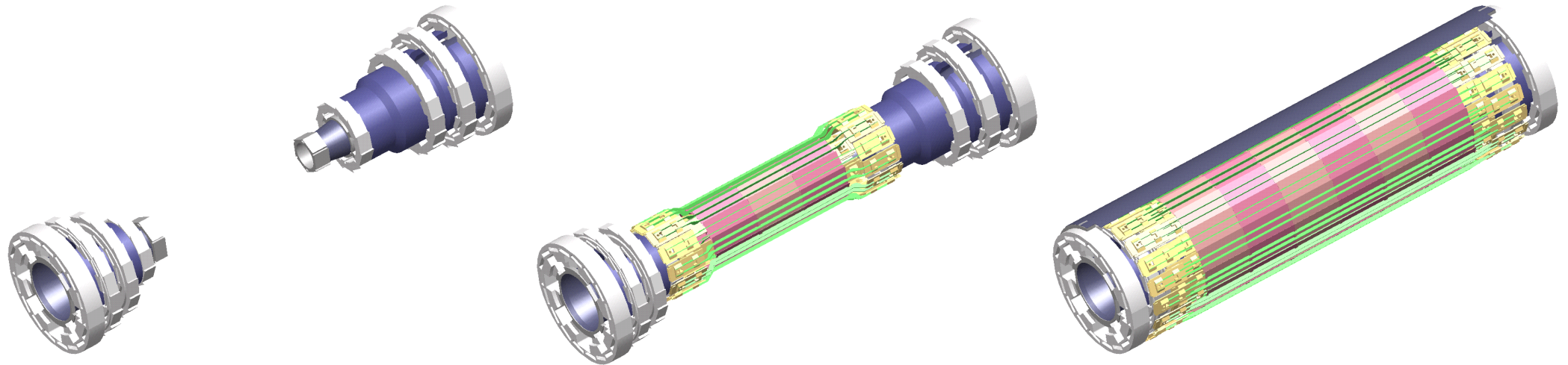


200 us

Mechanical structure of SVD2

Same concept with SVD1 (clam shell design)

- **more ladders** (32 \Rightarrow 54)
- Endrings : aluminum rings + **CFRP cones** (CTE ~ a few ppm)
- Longer/larger CFRP outer cover
- Heavier beam pipe (but independently supported by CDC)



3. Upgrade: SVD3?

KEKB($L \sim 10^{34}$) \Rightarrow Super-KEKB($L \sim 10^{35}$)

- New phase of physics:

- more full-reconstruction efficiency

- more background-rejection for rare decay

\rightarrow Better vertex resolution \rightarrow smaller($R_{bp} \sim 1\text{cm?}$) beam pipe

- Higher beam current:

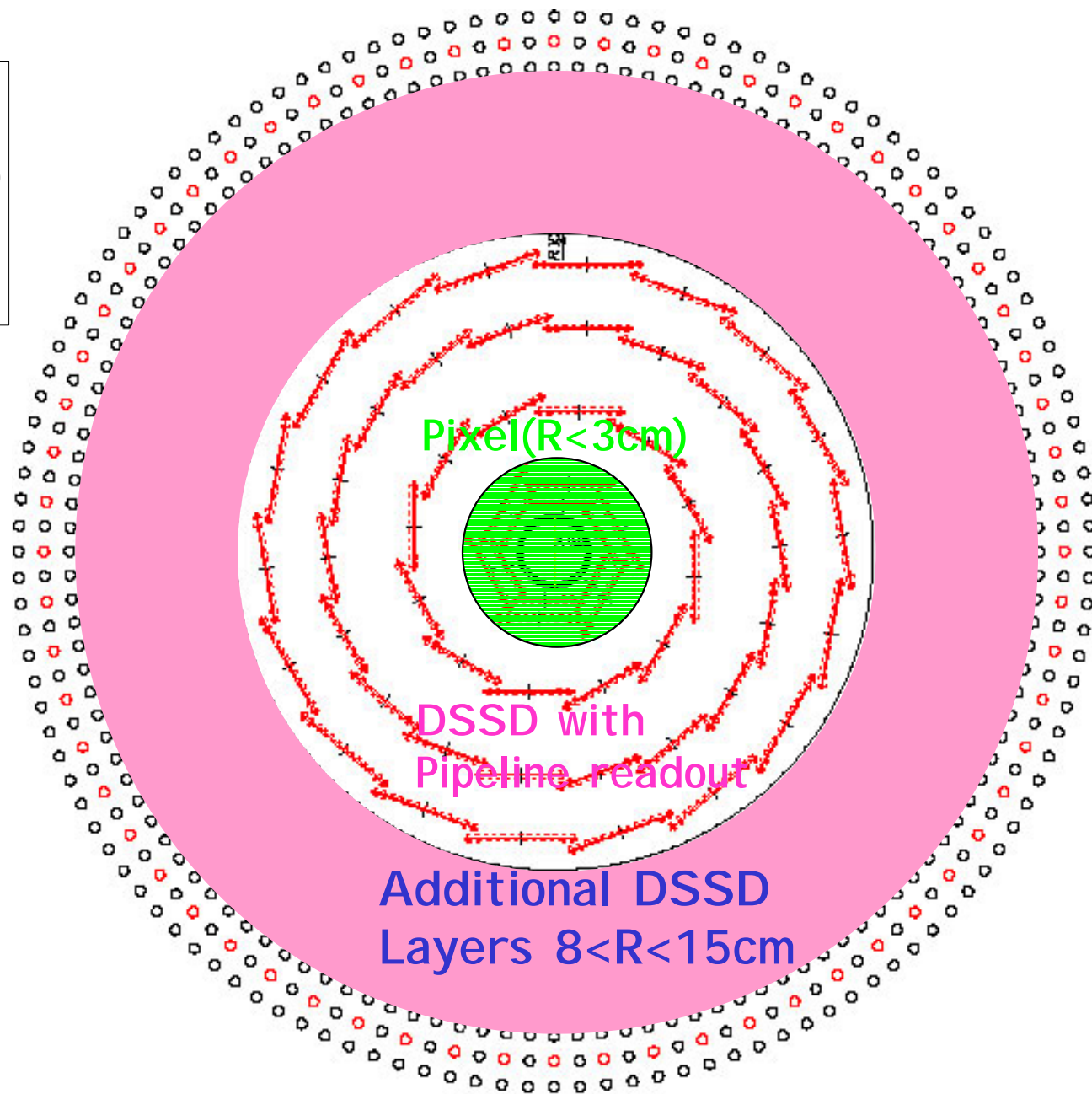
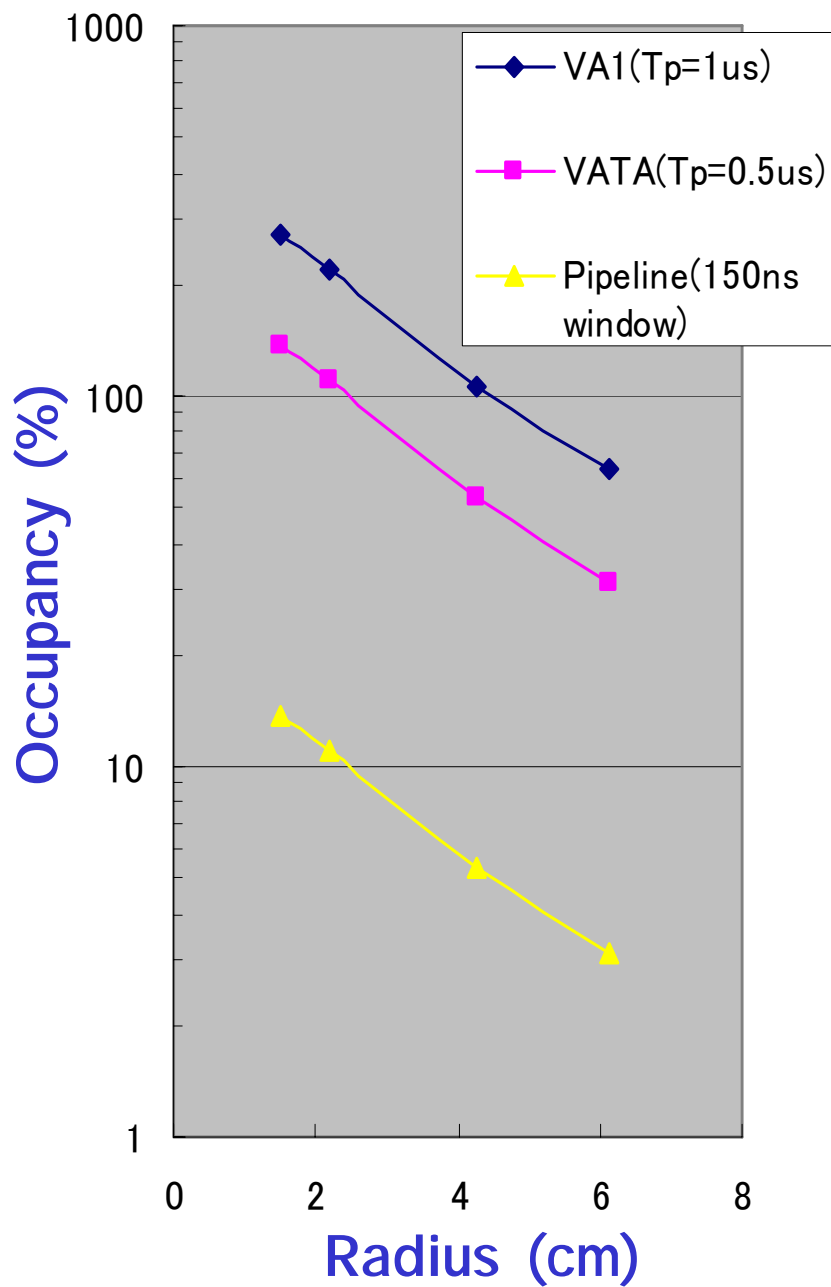
$2.6\text{A(LEP)} + 1.1\text{A(HER)} \Rightarrow 10\text{A(LEP)} + 4\text{A(HER)}$

$\rightarrow 0.2\text{MRad/year}@R_{bp} \sim 1.5\text{cm} \Rightarrow 7\text{MRad/year}@R_{bp} \sim 1.0\text{cm}$

$\rightarrow 1^{\text{st}}$ layer occupancy : 3% $\Rightarrow >100\%$ for DSSD

Pixel detector for inner layer
of new vertex detector (SVD3?)

Configuration of SVD3?



4. Summary

- We are constructing the new detector **SVD2**:
 - 3 layers: $R=3.0, 4.5, 6.0$ cm
 - ⇒ 4 layers: $R=2.0, 4.4, 7.0, 8.8$ cm
 - New DSSD ladder and repeater system
 - Floating DC operation and FLEX readout
 - More radiation hardness
 - $VA1-0.8\mu\text{m} : 1 \text{ MRad} \Rightarrow VA1-0.35\mu\text{m} : >20 \text{ MRad}$
 - Better trigger capability
 - $VA1 \rightarrow VA1TA$ (VA1 with trigger)
 - L-1.5 trigger in FADC system
 - Will be installed summer 2002?
- We have started to design **the Vertex Detector for Super-KEKB**